Armadillo-400 Series Hardware Manual

Version 1.7.0
2012/02/29

Atmark Techno, Inc.

Armadillo Site

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Chapter 1. Preface

The Armadillo Series is a line of small high-performance low-power general purpose boards which incorporate ARM CPU cores. Linux (kernel 2.6) is employed as the standard operating system, providing access to a rich array of software resources and proven stability. All boards include network interfaces as standard which, combined with the Linux network protocol stack, enable simple development of network ready devices.

The Armadillo-400 Series models provide improved performance over existing products of the same class, while at the same time also offering even lower power consumption. The Armadillo-400 Series is comprised of three products: the low cost Armadillo-420, the Armadillo-440 which can readily support multimedia functionality with the addition of an expansion board, and the Armadillo-460 which offers a high degree of expansion functionality.

Armadillo-400 Series boards have interfaces which are often required for embedded devices, such as serial, Ethernet, USB, storage (SD) and GPIO. In addition to these, multimedia functionality including LCD, touch screen and audio interfaces can be added to Armadillo-440 via an expansion board. On top of all this Armadillo-460 offers a high degree of expansion functionality by adding a SD slot with SDIO support, an expansion bus with a signal layout that conforms to PC/104 and also includes a real-time clock as standard.

The set models available in the Armadillo-400 Series are: the "Armadillo-420 Basic Model Development Set", the "Armadillo-420 WLAN Model Development Set", the "Armadillo-440 LCD Model Development Set" and the "Armadillo-460 Basic Model Development Set".

With the Armadillo-400 Series additional functionality such as a real-time clock or Wireless LAN can be added by utilizing an Armadillo-400 Series option module or expansion board. The "Armadillo-420 Basic Model Development Set" model is a set comprising of an Armadillo-420 together with the Armadillo-400 Series RTC Option Module. The "Armadillo-420 WLAN Model Development Set" includes an Armadillo-420 together with the Armadillo-400 Series WLAN Option Module. The "Armadillo-440 LCD Model Development Set" includes an Armadillo-440 with the Armadillo-400 Series LCD Expansion Board. While the "Armadillo-460 Basic Model Development Set" is the Armadillo-460 development model.

This document covers the hardware specifications of the Armadillo-400 Series. For guidance on how to use the default software, please see the "Armadillo-420 Basic Model Development Set Start-up Guide", the "Armadillo-420 WLAN Model Start-up Guide", the "Armadillo-440 LCD Model Development Set Start-up Guide" and the "Armadillo-460 Basic Model Development Set Startup Guide". When customizing the software, please refer to the "Armadillo-400 Series Software Manual".

1.1. Document and Related Files Versions

For all manuals including this document and also all other related files such as source files and image files, we recommend using the newest version available. Before continuing with this document, please check the Armadillo Site (http://armadillo.atmark-techno.com) for information on the latest versions.

1.2. Document Structure

This document covers the following points of required information for using the Armadillo-400 Series boards.

- Hardware Overview
- Memory Map
- Interface Specifications
- Board Layout

- Expansion Boards / Option Modules
- Case

1.3. Icons

Icons are used in the following way in this document.

This is used for precautions.

This is used for helpful information.

Chapter 2. Precautions

2.1. Safety Precautions

In order to use this product safely, please take special note of the following precautions.

- Be sure to read all product manuals and related documentation before using this product. Please use this product correctly and safely making sure to follow all usage precautions.
- When operating or extending this product in a way not described in the product manuals, please do so safely and on your own responsibility after having fully understood the materials on our web site and any other technical information.
- Please do not install this product in a place with a lot of water, moisture, dust or soot. This could cause a fire, product failure or electric shock.
- Some parts of this product generate heat and can reach high temperatures. Depending on the surrounding temperature and on how this product is handled, this may cause burns. Please do not touch the electronic components or the surrounding area while the product is powered on or before it has cooled down after being powered off.
- When using this product in the development of devices or systems to original specifications, please carry out the design and development after having thoroughly read and fully understood the product manuals and related materials, the technical information offered on our web site and related device data sheets. Also, please carry out full tests beforehand in order to provide and maintain reliability and safety.
- This product is not intended for uses that require extremely high reliability and safety in terms of functionality and accuracy (such as medical equipment, traffic control systems, combustion control systems, safety equipment and so on). If this product is used in these kinds of equipment, devices or systems, this company will not be held responsible in any way for any accident resulting in injury or death, fire or damage and so on.
- This product uses semiconductor components designed for generic electronics equipment such as office automation equipment, communications equipment, measurement equipment and machine tools. It is possible that a foreign noise or surge may cause this product to malfunction or fail. To ensure there will be no risk to life, the body or property in the event of malfunction or failure, be sure to take all possible measures in regard to device safety design, such as using protection circuits like limit switches or fuse breakers, or system redundancy, and to only use the device after taking measures to ensure sufficient reliability and safety.

- Please do not use products with Wireless LAN functionality in places near medical devices such as heart pacemakers and hearing aids, automatic control equipment such as fire alarms and automatic doors, microwave ovens, advanced electronic equipment or televisions and radios, or near "Premises Radio Stations" for "Mobile Body Identification" or "Specified Low Power Radio Stations". The radio waves emitted by this product may cause these types of devices to malfunction.

2.2. Handling Precautions

Please pay attention to the following points when handling this product in order to avoid causing any irreversible damage.

Areas Easily Damaged	The microSD connector and its cover and the connectors of the flat cable from Armadillo-440 and Armadillo-460 to the LCD Expansion Board can be easily damaged. Please be careful not to damage them by handling them with too much force.
Modifications To This Product	Please take note that any modifications[1] made to this product are not covered under warranty. Also, please ensure to undertake a full operational check of this product before carrying out any modifications or mounting connectors[2].
Mounting and Dismounting of Connectors While Powered On	Apart from hot-pluggable interfaces (LAN, USB, SD, Mic, Headphone), do not under any circumstances insert or remove connectors while power is supplied to this product or peripheral circuits.
Static Electricity	As CMOS devices are used in this product, please store it in antistatic packaging (such as that it was shipped in) until time of use.
Latch-up	Excessive noise or a surge from the power supply or input/output, or sharp voltage fluctuations can lead to the CMOS devices incorporated in the board causing a latch-up. Once the latch-up occurs, this situation continues until the power supply is disconnected, and therefore can damage the devices. Measures such as adding a protection circuit to noise-susceptible input/output lines or not sharing the power supply with devices that can be the cause of noise are highly recommended.
Physical Stress	Please avoid strong physical stress such as drops or other impacts.
Touch Panel Operation	The touch panel LCD module on the LCD expansion board is fixed with flexible double sided tape. If a strong force is applied to the LCD screen the double sided tape may give and the LCD frame may touch the board wiring. Please take care not to push the LCD screen stronger than necessary.

2.3. Software Usage Precautions

About Software Contained In This Product	The software and documentation contained in this product is provided “AS IS”. The customer is required to assume the responsibility of only using this product after having fully considered and tested its suitability to the intended purpose and use. There is no guarantee of fitness for a particular purpose, reliability, correctness and no guarantee of any outcomes resulting from the use of this product.

[1] With the exception of any methods of modification introduced in this and related product manuals, and the mounting of connectors to unmounted interfaces.
[2] When making modifications or mounting connectors, please ensure to apply masking and avoid solder residue or solder balls coming in contact with surrounding parts.

2.4. Write Prohibited Regions

The data stored by the EEPROM, CPLD and i.MX257 electrical fuse (e-Fuse) is used by the software contained in this product. Please do not write to these regions as the product may stop operating correctly. Purposefully writing to these regions voids the product warranty.

2.5. Electromagnetic Interference

The Armadillo-400 Series are Class A Information Technology Equipment[3] as defined under VCCI Council standards. There are cases where this type of equipment can cause electromagnetic interference when used in home environments. In this situation, the user may be required to take appropriate measures to alleviate the problem.

The Armadillo-440 LCD Model (Armadillo-440 together with the Armadillo-400 Series LCD Expansion Board fixed on an acrylic board) does not meet the VCCI standard and can cause electromagnetic interference.

In order to clear Class A when using the Armadillo-400 Series LCD Expansion Board included in the Armadillo-440 LCD Model, it is necessary to strengthen the ground of the expansion board. For example, by using a metal instead of acrylic board or connecting the fixing holes of the Armadillo-440 and the LCD Expansion Board with a wide conducting line.

Please be aware of the following points when newly designing an expansion board which connects to the LCD interface on Armadillo-440 or Armadillo-460.

With an expansion board that includes a device that has large power use fluctuations, such as with an audio amp, when only the GND line of the flexible flat cable (FCC) is connected the expansion board may produce electromagnetic noise. To mitigate the noise, strengthening of the expansion board's ground is recommended. For example, by connecting the fixing holes of the Armadillo-440 or Armadillo-460 and the expansion board GND by metal plate or wide conducting line.

2.6. Warranty

As laid out in the Product Warranty Policy which is provided with this product or available on our web site, the main board of this product is covered by a one year replacement warranty from time of purchase. Please note that the other included goods and software are not covered by the warranty.

[3] Armadillo-420, Armadillo-440 and Armadillo-460 have cleared Class A when tested with the AC adapter included in the Development Set (UNIFIVE US300520).

Product Warranty Policy http://www.atmark-techno.com/support/warranty-policy

2.7. Exporting

This product has as a general rule been developed and manufactured with the assumption that it will be used within Japan. When exporting this product, it is the responsibility of the exporter to follow all export related law and carry out all required procedures. No guarantee is made in regards to whether or not this product conforms to any overseas laws or regulations. This product and related technology may not be used for the purpose of development of weapons of mass destruction, for the purpose of military use or other military related uses, or in devices which have had their production, use, sale or procurement prohibited by national or overseas law or regulations.

2.8. Trademarks

- Armadillo is a registered trademark of Atmark Techno, Inc. All other company names, product names and related trademarks are the property of their respective owners. ™ and ® marks are omitted.
- The SD, SDHC, microSD, microSDHC and SDIO logos are trademarks of SD-3C, LLC.

Chapter 3. Overview

3.1. Board Overview

The main specifications of the Armadillo-400 Series are as follows.

Table 3.1. Armadillo-400 Series Board Specifications

	Armadillo-420	Armadillo-440	Armadillo-460
Processor	Freescale i.MX257 (MCIMX257)		
Processor	ARM926EJ-S Core Instruction / Data Cache: 16KByte / 16KByte Internal SRAM: 128KByte Thumb code (16bit instruction set) support		
System Clock	CPU Core Clock: 400MHz BUS Clock: 133MHz Oscillator Clock: 32.768kHz, 24MHz		
RAM	LPDDR SDRAM: 64MByte (16bit width) Micron MT46H32M16LFBF-6 IT or Samsung K4X51163PG-FGC6	LPDDR SDRAM: 128MByte (16bit width) Micron MT46H64M16LFCK-6 IT or Samsung K4X1G163PE-FGC6	
Flash Memory	NOR Flash Memory: 16MByte (16bit width) Numonyx PC28F128P30BF Maximum Write Cycles: 100,000 times	NOR Flash Memory: 32MByte (16bit width) Numonyx PC28F256P30BF Maximum Write Cycles: 100,000 times	
LAN (Ethernet)	10BASE-T/100BASE-TX with AUTO-MDIX		
Serial (UART)	3 channels max[a] UART2: • RS232C level • flow control pins (CTS,RTS,DTR, DSR,DCD,RI) • Max data transmission rate 230.4kbps UART3[b]/UART5[b]: • +3.3V CMOS Levels • flow control pins (CTS, RTS) • Max data transmission rate 4Mbps	4 channels max[a] UART2: • RS232C level • flow control pins (CTS,RTS,DTR, DSR,DCD,RI) • Max data transmission rate 230.4kbps UART3[b]/UART4[c]/UART5[b]: • +3.3V CMOS Levels • flow control pins (CTS, RTS) • Max data transmission rate 4Mbps	4 channels max[a] UART2 / UART4[d]: • RS232C levels • flow control pins UART2 (CTS,RTS,DTR, DSR,DCD,RI) UART4 (CTS,RTS) • Max data transmission rate 230.4kbps UART3[b] / UART4[c] / UART5[b]: • +3.3V CMOS Levels • flow control pins (CTS, RTS) • Max data transmission rate 4Mbps

	Armadillo-420	Armadillo-440	Armadillo-460
USB	2 channels (USB2.0, Host) USBOTG (USBPHY1): • High Speed support • Type-A connector (lower) USBHOST (USBPHY2): • Full Speed support • Type-A connector (upper)		2 channels (USB2.0, Host) USBOTG (USBPHY1): • High Speed support • Type-A connector (CON5) USBHOST (USBPHY2): • Full Speed support • Type-A connector (CON17)
SD/MMC	2 channels max[a] SDHC1: microSD slot SDHC2[b]: pin header		2 channels max[a] SDHC1: SD slot SDHC2[b]: pin header
Video	-	LCD Expansion I/F Max resolution: SVGA (800x600), 18bpp Connector Type: 50 pin FFC connector (0.5mm pitch)	
Touch Panel	-	4-Wire Resistive	
Audio I2S	1 channel max[a] (AUD6[b])	2 channels max[a] (AUD5[c], AUD6[b])	
I2C	1 channel max[a] (I2C2[e])	2 channels max[a] (I2C2[e], I2C3[c])	
SPI	2 channels max[a] (CSPI1[b], CSPI3[b])	2 channels max[a] (CSPI1[b], CSPI3[b])	
GPIO	24bit max[a]	35bit max[a]	35bit max[a]
Expansion Bus	-		Signal Layout PC/104 compliant (16bit)
Calendar Clock	None[f]		Real-time clock x1 Seiko Instruments Inc. RTC S-35390A equipped[g]
RTC Back-up Power	None[f]		300 sec (typ.), 60 sec (min.)[h] RTC External Backup Connector External battery can be connected via (CON13, CON20)
Switch	Tact Switch x1		Tact Switch x1 Reset Switch x1
LED	LED (red, ϕ3mm) x 1 LED (green, ϕ3mm) x 1 LED (yellow, surface mount) x 1		LED (red, surface mount) x 1 LED (green, surface mount) x 1 LED (yellow, surface mount) x 1
JTAG	8 pin (2.54mm pitch)[i]		
Power Supply Voltage	DC3.1 - 5.25V[j][k]		DC4.75V - 5.25V
Power Consumption	1.2W approx.[l]	1.2W approx. (Armadillo-440 only)[l] 2.0W approx. (Armadillo-440 with Armadillo-400 Series LCD Expansion Board)[l]	1.2W approx. (Armadillo-460 only)[l] 2.0W approx. (Armadillo-460 with Armadillo-400 Series LCD Expansion Board)[l]
Operating Temperature	-20 - 70℃ (with no condensation)		
Board Size	75.0 x 50.0mm (excluding protrusions)		90.2 × 95.9mm (excluding protrusions)
MTBF[m]	2.5 years approx.	2.4 years approx.	1.9 years approx.

[a]This is the number of channels available when the signal multiplex function on the i.MX257 is configured giving the most priority to this function.

[b]It is possible to assign this function to Expansion Interface 1 (CON9) with the signal multiplex function on i.MX257.

[c]It is possible to assign this function to the LCD Interface (CON11) with the signal multiplex function on i.MX257.

[d]Can be used exclusively of the LCD interface (CON11) signals with CPLD registers.

[e]It is possible to assign this function to Expansion Interface 2 (CON14) with the signal multiplex function on i.MX257.

[f]Can be added by connecting the Armadillo-400 Series RTC Option Module or the Armadillo-400 Series LCD Expansion Board.

[g]The time accuracy is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

[h]As backup time is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

[i]It is possible to convert this interface to the standard ARM 20 pin layout with the Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00) option. For details, please see Appendix A, Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00).

[j]When operating on a voltage less than 4.75V, please select the +5V generated by the PMIC for the USB power supply. There are certain limits to USB device supply current under these conditions. Please see Section 5.3.4, “CON5, CON6 (USB Interface) - Armadillo-420/440” for more details.

[k]When using the +5V produced by the PMIC for the USB power supply, please use within the range of VIN=DC3.1 - 4.8V. When using VIN > 4.8V, please use VIN instead of the +5V from the PMIC for the USB power supply.

[l]Does not include USB and SD device power consumption.

[m]Calculation based on MIL-HDBK-217F (NOTICE 2). Conditions: Ground Mobile, Ta=25℃.

3.2. Armadillo-420/440

3.2.1. Block Diagram - Armadillo-420/440

The Armadillo-420/440 block diagram is shown below.

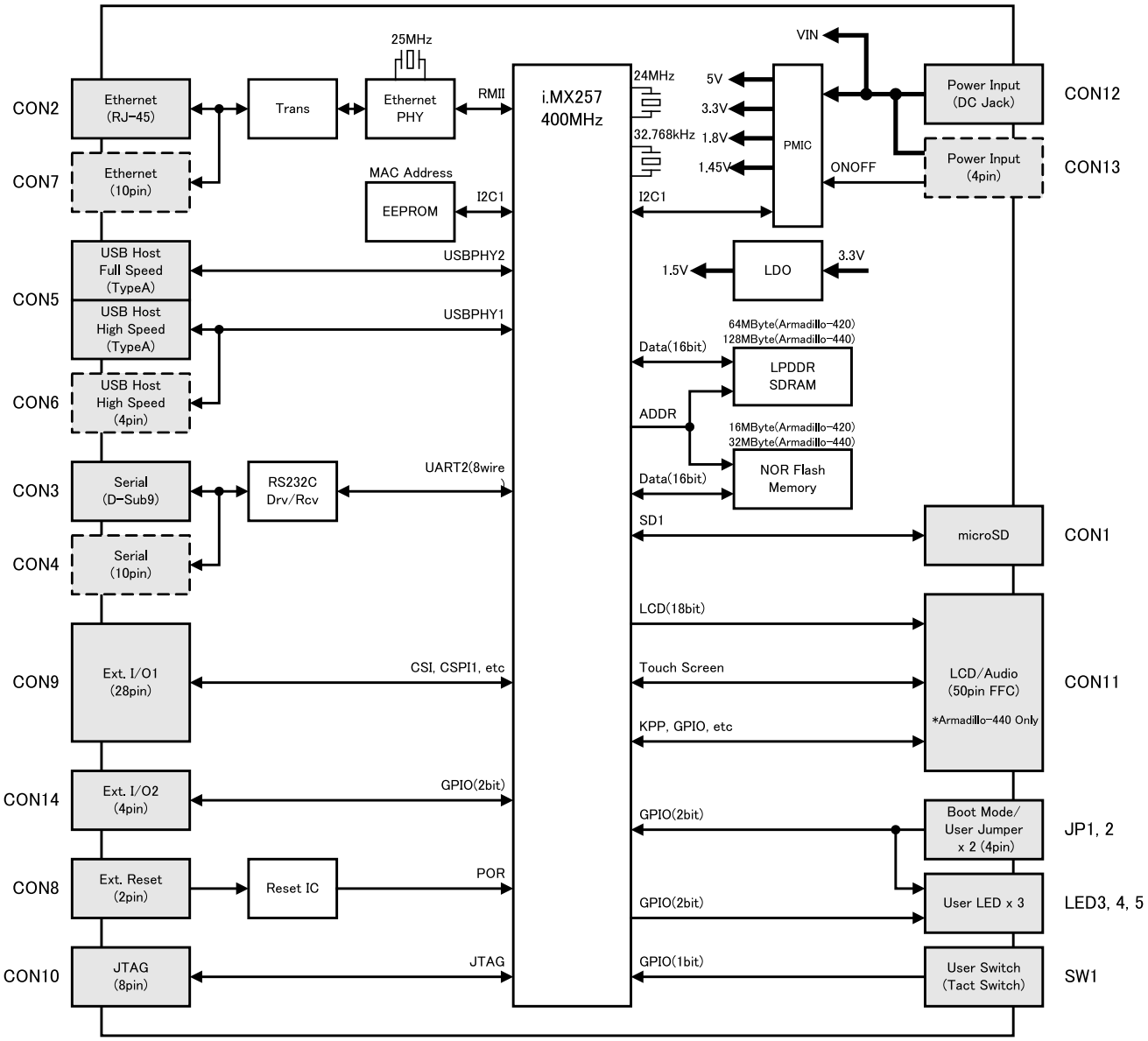


Figure 3.1. Armadillo-420/440 Block Diagram

3.2.2. Power Circuit Make-up - Armadillo-420/440

The power circuit make-up of Armadillo-420/440 is shown in Figure 3.2, “Armadillo-420/440 Power Circuit Make-up Diagram”.

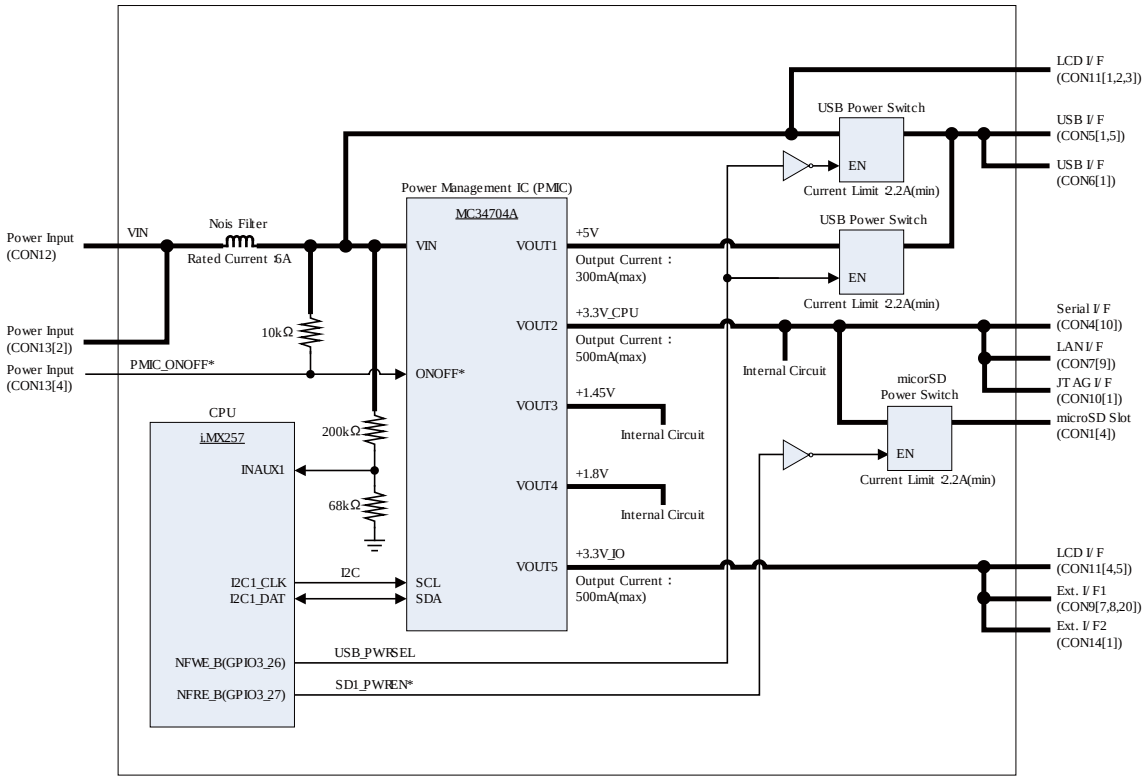


Figure 3.2. Armadillo-420/440 Power Circuit Make-up Diagram

With Armadillo-420/440, power input voltage from CON12 is converted to each required voltage by the power management IC (PMIC) and supplied to each interface and the internal circuits. Please ensure that the current capacity limit of each device is not exceeded when connecting external devices and configuring the power supply.

It is possible to select between the power in VIN of CON12 (or CON13) and the +5V power generated by the power management IC (PMIC) as the source of power provided to USB devices from the USB interfaces on Armadillo-420/440. When using a power input of less than 4.75V while connecting USB devices, please select the PMIC generated +5V power source. Please be aware that the total maximum current that can be supplied to the two USB channels is 300mA when using the PMIC generated +5V power source. The USB power source can be selected with the NFWE_B (GPIO3_26) pin on the i.MX257. The power in VIN is supplied when the NFWE_B (GPIO3_26) pin is low and the PMIC generated +5V supplied when it is high.

Armadillo-420/440 can be powered off by shorting the PMIC_ONOFF* signal to GND for more that two seconds. On power off the output voltage from the power management IC (PMIC) turns off. If PMIC_ONOFF* is once again shorted to GND in this state the PMIC will detect the falling edge and its power will turn back on, causing Armadillo-420/440 to start booting.

A zener diode is used from CON12 to the PMIC on Armadillo-420/440 for over-voltage protection.

As there is no overcurrent protection device such as a fuse between CON12 and the PMIC, please externally implement any overcurrent protection measures that may be necessary. Please be certain of the safety design of the device and only use it after taking full measures to ensure reliability and the maintenance of safety.

3.2.3. Power Sequence - Armadillo-420/440

The power sequence of Armadillo-420/440 is shown in Figure 3.3, “Armadillo-420/440 Power Sequence”.

The power on timing of the +3.3V_IO and +5V lines can be determined by controlling the power management IC (PMIC) via I2C.

T1 and T2 in Figure 3.3, “Armadillo-420/440 Power Sequence” and Figure 3.6, “Armadillo-460 Power Sequence” represent arbitrary timing values.

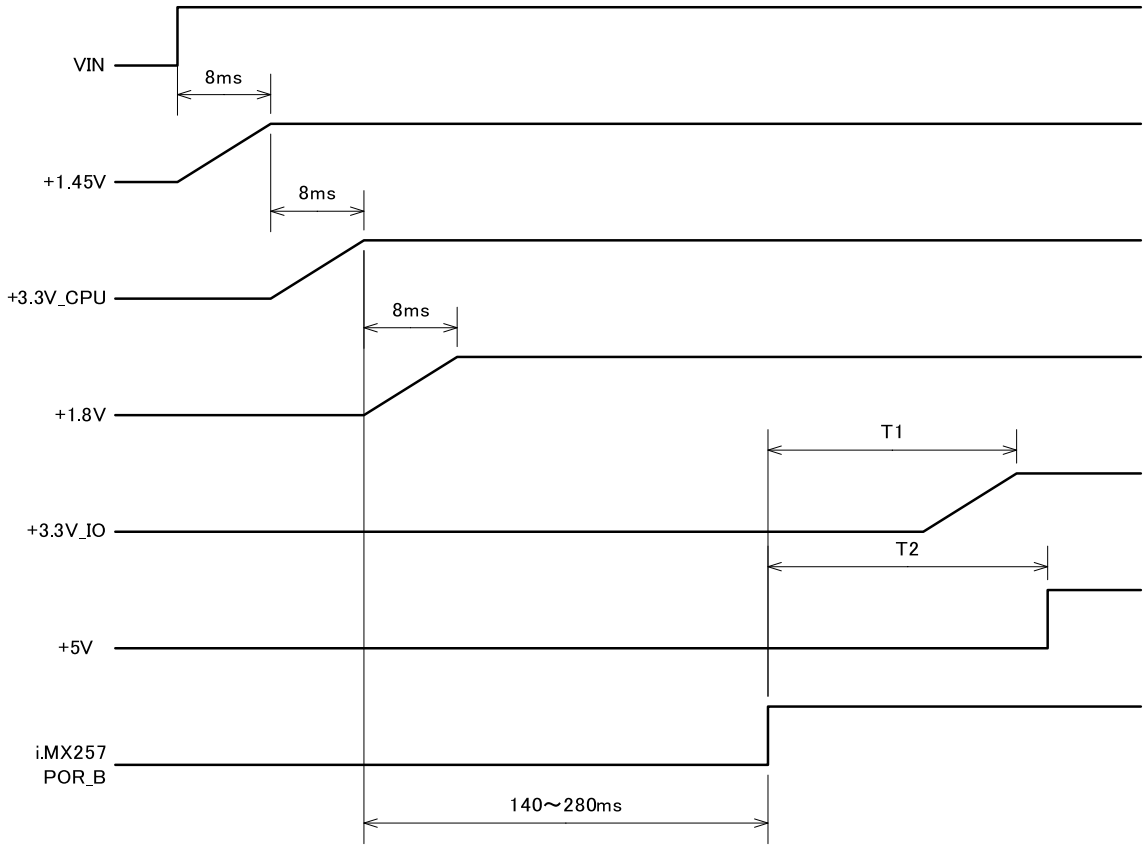


Figure 3.3. Armadillo-420/440 Power Sequence

3.3. Armadillo-460

3.3.1. Block Diagram - Armadillo-460

The Armadillo-460 block diagram is shown below.

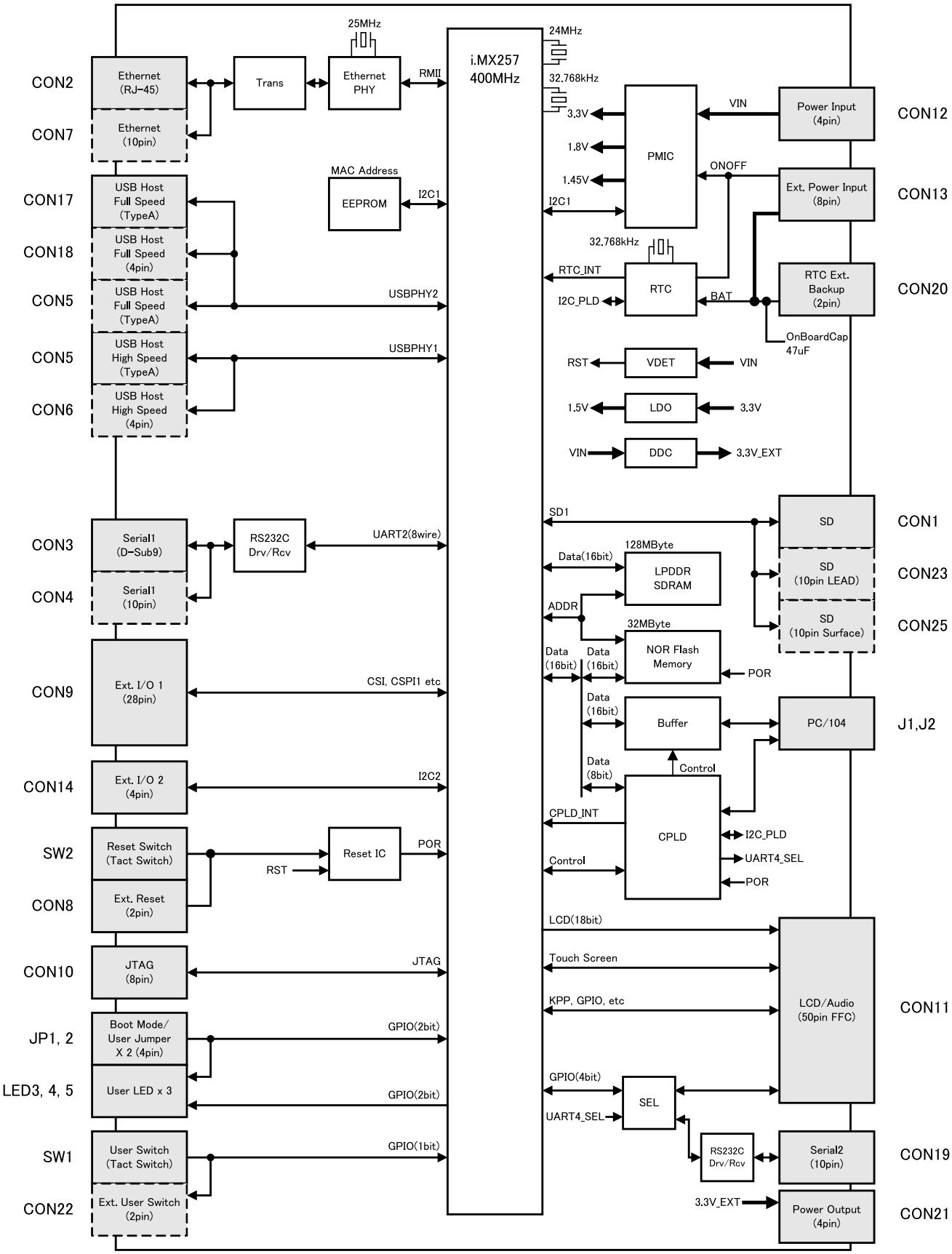


Figure 3.4. Armadillo-460 Block Diagram

3.3.2. Power Circuit Make-up - Armadillo-460

The power circuit make-up of Armadillo-460 is shown in Figure 3.5, “Armadillo-460 Power Circuit Make-up Diagram”.

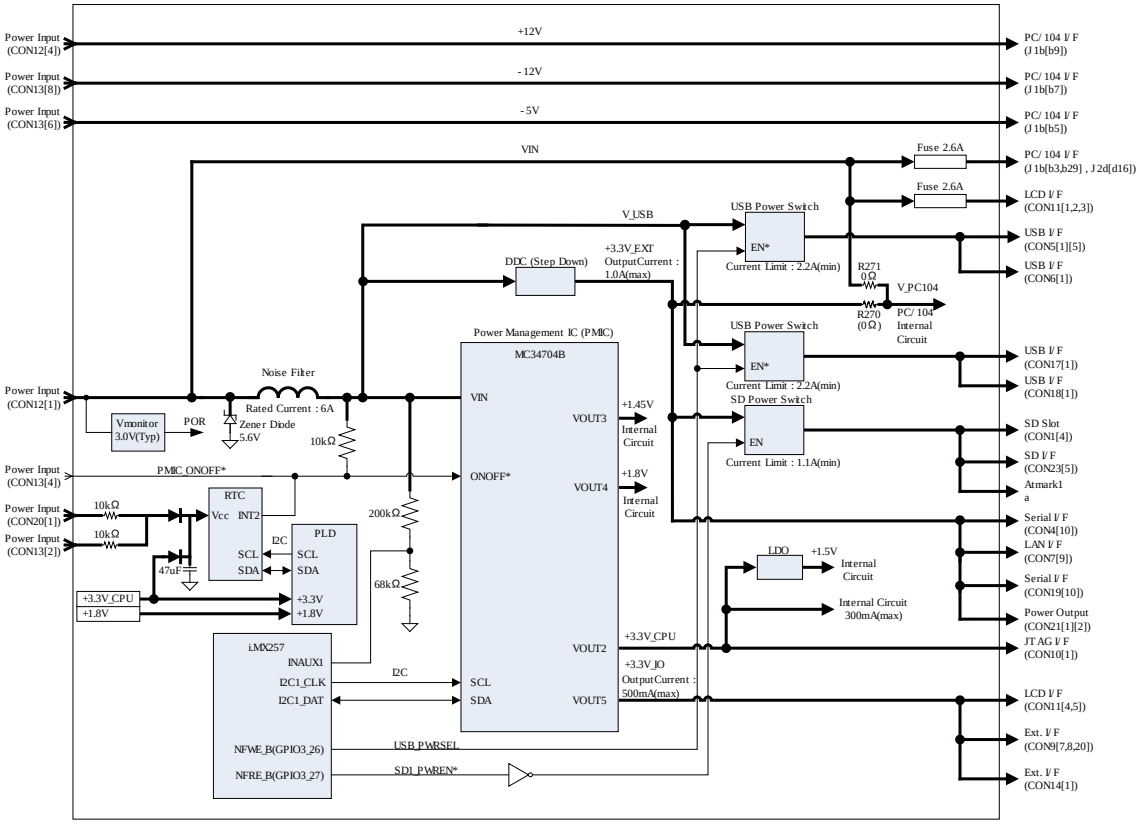


Figure 3.5. Armadillo-460 Power Circuit Make-up Diagram

With Armadillo-460, power input voltage from CON12 is converted to each required voltage by the power management IC (PMIC) and supplied to each interface and the internal circuits. Please ensure that the current capacity limit of each device is not exceeded when connecting external devices and configuring the power supply.

Aside from the PMIC Armadillo-460 has a step - down regulator. The +3.3V_EXT produced by the step - down regulator is supplied to the SD interface (CON1), the serial interfaces (CON4,CON19), the LAN interface (CON7) and the power output connector (CON21). Please note that the total max current supply is 1A.

Power in VIN of CON12 can be used as the source of power provided to USB devices from the USB interfaces on Armadillo-460. The USB power on/off can be selected with the NFWE_B (GPIO3_26) pin on the i.MX257. Power is supplied when the NFWE_B (GPIO3_26) pin is low and is not supplied when it is high.

Polyswitch fuses are included in J1/J2 and CON11 to prevent overcurrent between Armadillo-460 and an expansion board.

Either VIN or +3.3V_EXT can be selected for the V_PC104 power of the expansion bus interface. The V_PC104 selection is done by changing a chip resistor (0Ω). Please refer to Appendix D, Resistor Information - Armadillo-460 for information on how to make this switch.

Armadillo-460 can be powered off by shorting the PMIC_ONOFF* signal to GND for more that two seconds. On power off the output voltage from the power management IC (PMIC) turns off. If PMIC_ONOFF* is once again shorted to GND in this state the PMIC will detect the falling edge and its power will turn back on, causing Armadillo-460 to start booting.

A real-time clock (RTC) is included on Armadillo-460 as standard. By pre-configuring a time to alarm 2 of the RTC, it is possible to bring Armadillo-460 out of a power off state at the configured time by way of the PMIC_ONOFF* signal.

When using this functionality, it is recommended that a RTC backup power source (+3.3V) such as WK11 (Hitachi Maxell) is separately connected to CON20. Please note that while it is possible to power Armadillo-460 back on for approximately one minute after power off if the RTC backup 47uF condenser included as standard on Armadillo-460 has been fully charged by the internal +3.3V_CPU, if the power off state continues for longer than this and the voltage of the 47uF condenser falls, it will no longer be possible to power Armadillo-460 back on with alarm 2 of the RTC.

While a zener diode is included from CON12 to the PMIC on Armadillo-460 for over-voltage protection, as there is no overcurrent protection device such as a fuse between CON12 and the PMIC, please externally implement any overcurrent protection measures that may be necessary. Please be certain of the safety design of the device and only use it after taking full measures to ensure reliability and the maintenance of safety.

When using the expansion bus interface in direct CPU bus mode, please be sure to select +3.3V_EXT for V_PC104. Using VIN (+5V) for V_PC104 causes a large amount of radiation noise to be generated from the board.

A maximum of 1.6A can be assigned to the J1/J2 +5V power (b3,b29,d16) of the expansion bus on Armadillo-460. Please design the connecting PC/104 expansion board so that its total power consumption does not exceed 1.6A.

3.3.3. Power Sequence - Armadillo-460

The power sequence of Armadillo-460 is shown in Figure 3.6, “Armadillo-460 Power Sequence”.

The power on timing of the +3.3V_IO and +5V lines can be determined by controlling the power management IC (PMIC) via I2C.

T1 and T2 in Figure 3.3, “Armadillo-420/440 Power Sequence” and Figure 3.6, “Armadillo-460 Power Sequence” represent arbitrary timing values.

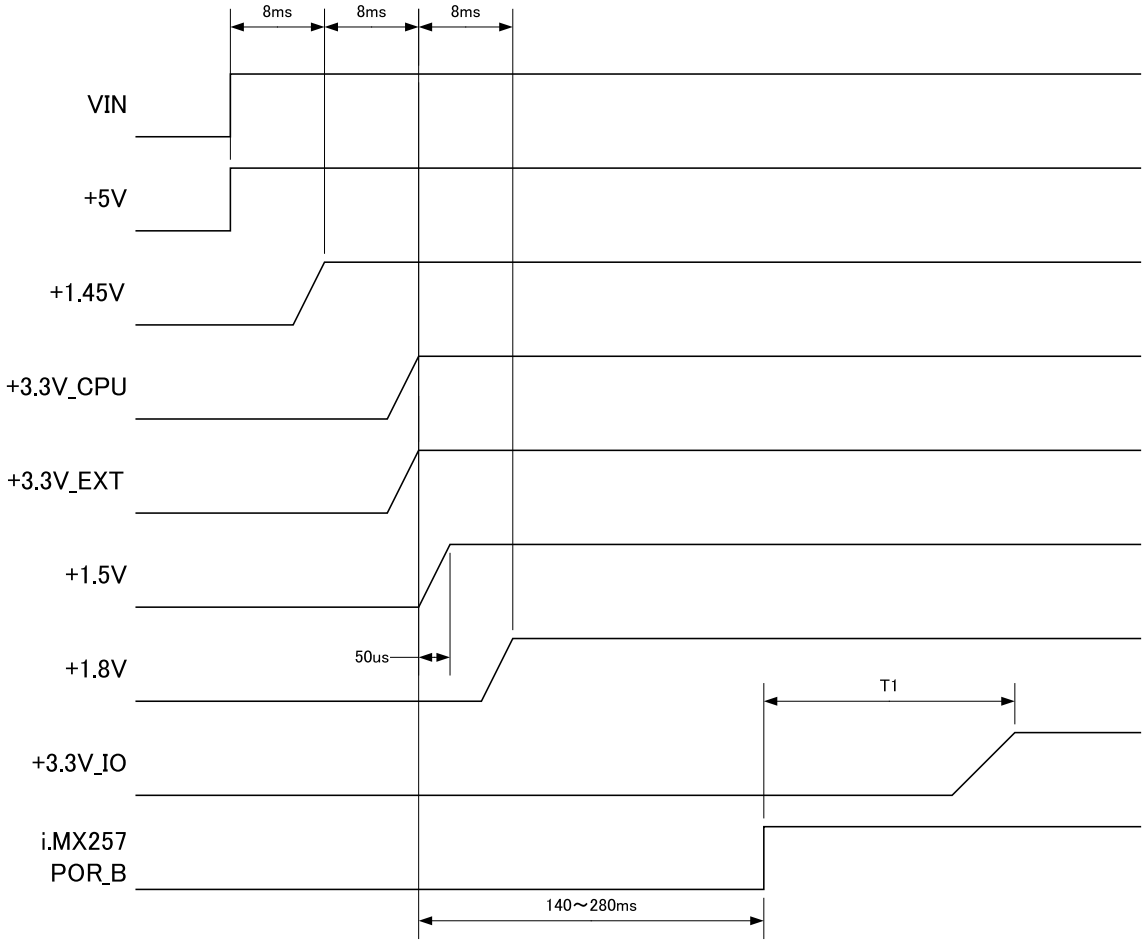


Figure 3.6. Armadillo-460 Power Sequence

Chapter 4. Memory Map

4.1. Armadillo-420/440

4.1.1. Physical Memory Map - Armadillo-420/440

The physical memory map of Armadillo-420/440 is as shown.

Table 4.1. Physical Memory Map - Armadillo-420/440

Start Address	End Address	Armadillo-420	Armadillo-440	Memory Area	Data Port Width
0x0000 0000	0x0000 3FFF	i.MX257 Internal ROM (16KByte)			
0x0000 4000	0x0040 3FFF	Reserved			
0x0040 4000	0x0040 8FFF	i.MX257 Internal ROM (20KByte)			
0x0040 9000	0x3FFF FFFF	Reserved			
0x4000 0000	0x6FFF FFFF	i.MX257 Internal Register[a]			
0x7000 0000	0x77FF FFFF	Reserved			
0x7800 0000	0x7801 FFFF	i.MX257 Internal RAM (128KByte)			
0x7802 0000	0x7FFF FFFF	Reserved			
0x8000 0000	0x83FF FFFF	LPDDR SDRAM (64MByte)	LPDDR SDRAM (128MByte)	CSD0	16bit
0x8400 0000	0x87FF FFFF	Reserved			
0x8800 0000	0x8FFF FFFF	Reserved			
0x9000 0000	0x9FFF FFFF	Reserved		CSD1	
0xA000 0000	0xA0FF FFFF	NOR Flash Memory (16MByte)	NOR Flash Memory (32MByte)	CS0	16bit
0xA100 0000	0xA1FF FFFF	Reserved			
0xA200 0000	0xA7FF FFFF	Reserved			
0xA800 0000	0xA800 000F	Reserved		CS1	8bit
0xA800 0010	0xA800 00FF				
0xA800 0100	0xAFFF FFFF	Reserved			
0xB000 0000	0xB1FF FFFF	Reserved		CS2	
0xB200 0000	0xB200 FFFF	Reserved		CS3	
0xB201 0000	0xB2FF FFFF				
0xB300 0000	0xB3FF FFFF				
0xB400 0000	0xB400 FFFF	Reserved		CS4	
0xB401 0000	0xB4FF FFFF				
0xB500 0000	0xB57F FFFF				
0xB580 0000	0xB5FF FFFF				
0xB600 0000	0xB800 0FFF	Reserved			
0xB800 1000	0xBB00 1FFF	i.MX257 Internal Register[a]			
0xBB01 2000	0xBFFF FFFF	Reserved			
0xC000 0000	0xFFFF FFFF	Reserved			

[a]For details on the internal registers on the i.MX257, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

4.2. Armadillo-460

4.2.1. Physical Memory Map - Armadillo-460

The physical memory map of Armadillo-460 is as shown.

Table 4.2. Physical Memory Map - Armadillo-460

Start Address	End Address	Armadillo-460		Memory Area	Data Port Width
		PC/104 Expansion Bus Mode	Direct CPU Bus Mode		
0x0000 0000	0x0000 3FFF	i.MX257 Internal ROM (16KByte)			
0x0000 4000	0x0040 3FFF	Reserved			
0x0040 4000	0x0040 8FFF	i.MX257 Internal ROM (20KByte)			
0x0040 9000	0x3FFF FFFF	Reserved			
0x4000 0000	0x6FFF FFFF	i.MX257 Internal Register[a]			
0x7000 0000	0x77FF FFFF	Reserved			
0x7800 0000	0x7801 FFFF	i.MX257 Internal RAM (128KByte)			
0x7802 0000	0x7FFF FFFF	Reserved			
0x8000 0000	0x83FF FFFF	LPDDR SDRAM (128MByte)		CSD0	16bit
0x8400 0000	0x87FF FFFF				
0x8800 0000	0x8FFF FFFF	Reserved			
0x9000 0000	0x9FFF FFFF	Reserved		CSD1	
0xA000 0000	0xA0FF FFFF	NOR Flash Memory (32MByte)		CS0	16bit
0xA100 0000	0xA1FF FFFF				
0xA200 0000	0xA7FF FFFF	Reserved			
0xA800 0000	0xA800 000F	CPLD Register		CS1	8bit
0xA800 0010	0xA800 00FF	Reserved			
0xA800 0100	0xAFFF FFFF	Reserved			
0xB000 0000	0xB1FF FFFF	Reserved		CS2	
0xB200 0000	0xB200 FFFF	PC/104 I/O Space 8bit	CS3 Access 8bit/ 16bit	CS3	
0xB201 0000	0xB2FF FFFF	Reserved			
0xB300 0000	0xB3FF FFFF	PC/104 Memory Space 8bit			
0xB400 0000	0xB400 FFFF	PC/104 I/O Space 16bit	CS4 Access 8bit/ 16bit	CS4	
0xB401 0000	0xB4FF FFFF	Reserved			
0xB500 0000	0xB57F FFFF	PC/104 Memory Space 16bit			
0xB580 0000	0xB5FF FFFF	Reserved			
0xB600 0000	0xB800 0FFF	Reserved			
0xB800 1000	0xBB00 1FFF	i.MX257 Internal Register[a]			
0xBB01 2000	0xBFFF FFFF	Reserved			
0xC000 0000	0xFFFF FFFF	Reserved			

[a] For details on the internal registers on the i.MX257, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

4.2.2. CS3/CS4 Space - Armadillo-460 (Direct CPU Bus Mode)

Table 4.3. CS3/CS4 Space Accessible in Direct CPU Bus Mode

<table>
<tr><th rowspan="2">Chip Select</th><th rowspan="2">Physical Address</th><th colspan="2">Synchronous Mode[a]</th><th colspan="4">Asynchronous Mode [b]</th></tr>
<tr><th>8bit[c]</th><th>16bit[d]</th><th>8bit[e]</th><th>8bit AUS[f]</th><th>16bit[g]</th><th>16bit AUS[h]</th></tr>
<tr><td rowspan="8">CS3</td><td>0xb2000000
|
0xb27fffff</td><td rowspan="2">16MByte</td><td>8MByte</td><td rowspan="2">16MByte</td><td>8MByte</td><td rowspan="4">32MByte</td><td>8MByte</td></tr>
<tr><td>0xb2800000
|
0xb2ffffff</td><td rowspan="3">Reserved</td><td rowspan="2">Reserved</td><td rowspan="3">Reserved</td></tr>
<tr><td>0xb3000000
|
0xb37fffff</td><td rowspan="2">Reserved</td><td rowspan="2">Reserved</td></tr>
<tr><td>0xb3800000
|
0xb3ffffff</td></tr>
<tr><td rowspan="8">CS4</td><td>0xb4000000
|
0xb47fffff</td><td rowspan="4">Reserved</td><td rowspan="4">Reserved</td><td rowspan="2">16MByte</td><td>8MByte</td><td rowspan="4">32MByte</td><td>8MByte</td></tr>
<tr><td>0xb4800000
|
0xb4ffffff</td><td rowspan="3">Reserved</td><td rowspan="3">Reserved</td></tr>
<tr><td>0xb5000000
|
0xb57fffff</td><td rowspan="2">Reserved</td></tr>
<tr><td>0xb5800000
|
0xb5ffffff</td></tr>
</table>

[a] When set to direct CPU bus mode (synchronous)
[b] When set to direct CPU bus mode (asynchronous)
[c] When data bus width is set to 8bit
[d] When data bus width is set to 16bit
[e] When data bus width is set to 8bit and AUS3/AUS4 bits in the WCR register of WEIM are not set to 1
[f] When data bus width is set to 8bit and AUS3/AUS4 bits in the WCR register of WEIM are set to 1
[g] When data bus width is set to 16bit and AUS3/AUS4 bits in the WCR register of WEIM are not set to 1
[h] When data bus width is set to 16bit and AUS3/AUS4 bits in the WCR register of WEIM not set to 1

Due to the Errata ENGcm11270 limitation, A[23] cannot be used when AUS (Address Unshifted mode) is specified. Because of this, the address space is restricted dependent on the direct CPU bus mode configuration. For information on this errata, please refer to "ENGcm11270" in "Chip Errata for the i.MX25" from the /document/datasheet/ directory on the included DVD.

Chapter 5. Interface Specifications - Armadillo-420/440

5.1. Interface Layout - Armadillo-420/440

5.1.1. Armadillo-420 Interface Layout

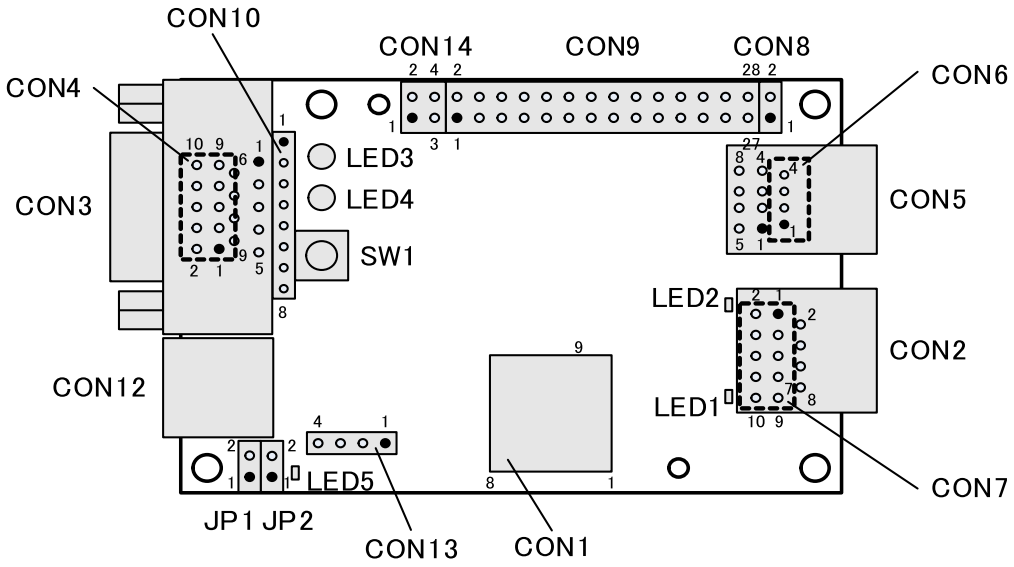


Figure 5.1. Armadillo-420 Interface Layout

Table 5.1. Armadillo-420 Interfaces[a]

Part Number	Interface	Shape	Notes
CON1	SD	microSD slot (hinge type)	
CON2	LAN	RJ-45 Connector	
CON3	Serial 1	D-Sub 9 pin (male)	
CON4	Serial 1	Pin headers (10P) (2.54mm pitch)	Signal lines shared with CON3
CON5	USB	Type-A connector (2 port stack)	
CON6	USB	Pin headers (4P) (2mm pitch)	Signal lines shared with lower port of CON5
CON7	LAN	Pin headers (10P) (2.54mm pitch)	Some signal lines shared with CON2
CON8	External Reset	Pin headers (2P) (2.54mm pitch)	
CON9	Expansion 1	Pin headers (28P) (2.54mm pitch)	
CON10	i.MX257 JTAG	Pin headers (8P) (2.54mm pitch)	
CON12	Power in	DC jack	

Part Number	Interface	Shape	Notes
CON13	Power in	Pin headers (4P) (2.54mm pitch)	
CON14	Expansion 2	Pin headers (4P) (2.54mm pitch)	
JP1	Boot mode jumper	Pin headers (2P) (2.54mm pitch)	
JP2	User jumper	Pin headers (2P) (2.54mm pitch)	
LED1	LAN Link LED	LED (green, surface mount)	Shown on upper part of CON2
LED2	LAN Activity LED	LED (yellow, surface mount)	Shown on upper part of CON2
LED3	User LED	LED (red, ϕ3mm)	
LED4	User LED	LED (green, ϕ3mm)	
LED5	User LED	LED (yellow, surface mount)	
SW1	User switch	Tact Switch (h=17mm)	

[a]Parts with a white part number background are equipped as standard. Parts with a gray part number background are not equipped as standard, but can be optionally added.

5.1.2. Armadillo-440 Interface Layout

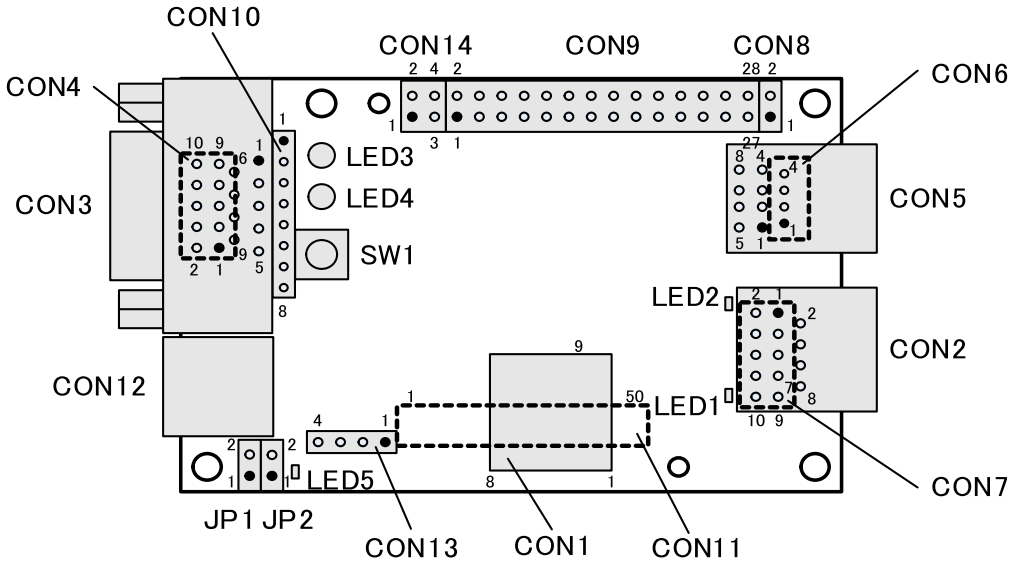


Figure 5.2. Armadillo-440 Interface Layout

Table 5.2. Armadillo-440 Interfaces[a]

Part Number	Interface	Shape	Notes
CON1	SD	microSD slot (hinge type)	
CON2	LAN	RJ-45 Connector	
CON3	Serial 1	D-Sub 9 pin (male)	
CON4	Serial 1	Pin headers (10P) (2.54mm pitch)	Signal lines shared with CON3
CON5	USB	Type-A connector (2 port stack)	
CON6	USB	Pin headers (4P) (2mm pitch)	Signal lines shared with lower port of CON5
CON7	LAN	Pin headers (10P) (2.54mm pitch)	Some signal lines shared with CON2

Part Number	Interface	Shape	Notes
CON8	External Reset	Pin headers (2P) (2.54mm pitch)	
CON9	Expansion 1	Pin headers (28P) (2.54mm pitch)	
CON10	i.MX257 JTAG	Pin headers (8P) (2.54mm pitch)	
CON11	LCD Expansion	FFC Connector (50P) (0.5mm pitch)	
CON12	Power in	DC jack	
CON13	Power in	Pin headers (4P) (2.54mm pitch)	
CON14	Expansion 2	Pin headers (4P) (2.54mm pitch)	
JP1	Boot mode jumper	Pin headers (2P) (2.54mm pitch)	
JP2	User jumper	Pin headers (2P) (2.54mm pitch)	
LED1	LAN Link LED	LED (green, surface mount)	Shown on upper part of CON2
LED2	LAN Activity LED	LED (yellow, surface mount)	Shown on upper part of CON2
LED3	User LED	LED (red, ϕ3mm)	
LED4	User LED	LED (green, ϕ3mm)	
LED5	User LED	LED (yellow, surface mount)	
SW1	User switch	Tact Switch (h=17mm)	

[a]Parts with a white part number background are equipped as standard. Parts with a gray part number background are not equipped as standard, but can be optionally added.

5.2. Electrical Specifications - Armadillo-420/440

5.2.1. Input/Output Interface Electrical Specifications - Armadillo-420/440

The rated absolute maximum of the input/output interface is shown in Table 5.3, “Input/Output Interface Rated Absolute Maximum - Armadillo-420/440”, the power supply specifications in Table 5.4, “Input/Output Interface Power Supply Electrical Specifications - Armadillo-420/440”, and the electrical specifications in Table 5.5, “Input/Output Interface Electrical Specifications - Armadillo-420/440”.

With the Software Pad Control (SW_PAD_CTL) and Drive Voltage Select Group Control (SW_PAD_CTL_GRP_DVS) registers in i.MX257 it is possible to alter the output current (Std, High, Max), slew rate (Slow, Fast), and pull-up/pull-down.

Table 5.3. Input/Output Interface Rated Absolute Maximum - Armadillo-420/440

Symbol	Parameter	Min	Max	Units
VImax	Input voltage range	–0.5	OVDD+0.3	V

Table 5.4. Input/Output Interface Power Supply Electrical Specifications - Armadillo-420/440

Symbol	Parameter	Min	Max	Units	Conditions
+3.3V_IO	Power Supply Voltage	0.95 x VDD_IO	1.05 x VDD_IO	V	VDD_IO = +3.3V
	Power Supply Current	-	0.5	A	

Table 5.5. Input/Output Interface Electrical Specifications - Armadillo-420/440

Symbol	Parameter	Min	Max	Units	Conditions
VIH	CMOS High-Level Input Voltage	0.7 x OVDD	OVDD	V	OVDD = +3.3V
VIL	CMOS Low-Level Input Voltage	-0.3	0.3 x OVDD	V	OVDD = +3.3V

Symbol	Parameter	Min	Max	Units	Conditions
VOH	CMOS High-Level Output Voltage	OVDD-0.15	-	V	IOH = -1mA
		0.8 x OVDD	-	V	IOH = Specified Drive
VOL	CMOS Low-Level Output Voltage	-	0.15	V	IOL = 1mA
		-	0.2 x OVDD	V	IOL = Specified Drive
IOH_S	High-Level Output Current, Slow Slew Rate	-2.0	-	mA	VOH = 0.8 x OVDD, Std Drive
		-4.0	-	mA	VOH = 0.8 x OVDD, High Drive
		-8.0	-	mA	VOH = 0.8 x OVDD, Max Drive
IOH_F	High-Level Output Current, Fast Slew Rate	-4.0	-	mA	VOH = 0.8 x OVDD, Std Drive
		-6.0	-	mA	VOH = 0.8 x OVDD, High Drive
		-8.0	-	mA	VOH = 0.8 x OVDD, Max Drive
IOL_S	Low-Level Output Current, Slow Slew Rate	2.0	-	mA	VOL = 0.2 x OVDD, Std Drive
		4.0	-	mA	VOL = 0.2 x OVDD, High Drive
		8.0	-	mA	VOL = 0.2 x OVDD, Max Drive
IOL_F	Low-Level Output Current, Fast Slew Rate	4.0	-	mA	VOH = 0.2 x OVDD, Std Drive
		6.0	-	mA	VOH = 0.2 x OVDD, High Drive
		8.0	-	mA	VOH = 0.2 x OVDD, Max Drive
IIN	Input Current (no PU/PD[a])	-	0.1	µA	VI = 0
		-	0.06	µA	VI = OVDD = +3.3V
	Input Current (22kΩPU)	117	184	µA	VI = 0
		0.0001	0.0001	µA	VI = OVDD = +3.3V
	Input Current (47kΩPU)	54	88	µA	VI = 0
		0.0001	0.0001	µA	VI = OVDD = +3.3V
	Input Current (100kΩPU)	25	42	µA	VI = 0
		0.0001	0.0001	µA	VI = OVDD = +3.3V
	Input Current (100kΩPD)	0.0001	0.0001	µA	VI = 0
		25	42	µA	VI = OVDD = +3.3V
ICC	High-impedance Supply Current	-	1.2	µA	VI = 0
		-	1.2	µA	VI = OVDD = +3.3V

[a]PU=Pull Up, PD=Pull Down

5.3. Interfaces - Armadillo-420/440

5.3.1. CON1 (SD Interface) - Armadillo-420/440

CON1 on Armadillo-420/440 is a microSD/microMMC slot. It is connected to the SD/MMC controller (SDHC1) on i.MX257.

Power supplied to the SD interface can be turned on and off with the NFRE_B (GPIO3_27) pin on i.MX257. After the NFRE_B (GPIO3_27) pin on i.MX257 is set to GPIO output mode, power supply will start on a low signal and stop on a high signal.

Table 5.6. CON1 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	SD1_DAT2	In/Out	Data bus (bit 2), connected to SD1_DATA2 pin on i.MX257

Pin Number	Signal Name	I/O	Function
2	SD1_DAT3	In/Out	Data bus (bit 3), connected to SD1_DATA3 pin on i.MX257
3	SD1_CMD	In/Out	Command / Response, connected to SD1_CMD pin on i.MX257
4	VDD	Power	Power (+3.3V_CPU)[a]
5	SD1_CLK	Out	Clock, connected to SD1_CLK pin on i.MX257
6	VSS	Power	Power (GND)
7	SD1_DAT0	In/Out	Data bus (bit 0), connected to SD1_DATA0 pin on i.MX257
8	SD1_DAT1	In/Out	Data bus (bit 1), connected to SD1_DATA1 pin on i.MX257
9	SD1_CD*	In	Card detect (low: card inserted, high: card ejected) connected to NFRB (GPIO3_31) pin on i.MX257

[a]The combined maximum output current of CON1, CON4, CON7 and CON10 is 200mA.

CON1 (microSD) on Armadillo-420/440 is a hinge type connector. The cover on the connector must be opened in order to insert and remove the card. When opening, the cover should first be unlocked by sliding the upper part of the connector horizontally in the directory shown by the OPEN arrow.

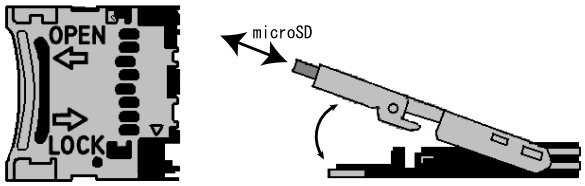


Figure 5.3. microSD Card Insertion and Removal - Armadillo-420/440

CON1 (microSD/microMMC) is not hot-pluggable. Be sure to turn off the power supply before inserting or removing a microSD card.

Please ensure to leave the cover on CON1 (microSD/microMMC) in a locked state, regardless of whether a microSD card is inserted or not. If the cover is left unlocked when a microSD is not inserted, the internal contact of the connector may come into contact with the cover and cause Armadillo-420/440 to reset.

Information on tested microSD / microMMC cards is available on the Armadillo Site and is updated regularly.

5.3.2. CON2, CON7 (LAN Interface) - Armadillo-420/440

CON2 and CON7 are a 10BASE-T/100BASE-TX LAN interface which can be used with Category 5 or above Ethernet cables. The interface includes AUTO-MDIX functionality allowing it to automatically detect straight or cross cable connections and swap the send and receive terminals accordingly.

Table 5.7. CON2 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	TX+	Out	Differential twisted pair transmit (+), signal line shared with CON7 (pin 1)
2	TX-	Out	Differential twisted pair transmit (-), signal line shared with CON7 (pin 4)
3	RX+	In	Differential twisted pair receive (+), signal line shared with CON7 (pin 3)
4	-	-	75Ω terminal after connection with CON2 (pin 5), signal line shared with CON7 (pin 5)
5	-	-	75Ω terminal after connection with CON2 (pin 4), signal line shared with CON7 (pin 5)
6	RX-	In	Differential twisted pair receive (-), signal line shared with CON7 (pin 6)
7	-	-	75Ω terminal after connection with CON2 (pin 8), signal line shared with CON7 (pin 7)
8	-	-	75Ω terminal after connection with CON2 (pin 7), signal line shared with CON7 (pin 7)

Table 5.8. CON7 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	TX+	Out	Differential twisted pair transmit (+), signal line shared with CON2 (pin 1)
2	ACTIVITY_LED	Out	Activity indicator (low: data transmit/receive, high: no data)
3	RX+	In	Differential twisted pair receive (+), signal line shared with CON2 (pin 3)
4	TX-	Out	Differential twisted pair transmit (-), signal shared with CON2 (pin 2)
5	-	-	75Ω terminal, signal line shared with CON2 (pins 4, 5)
6	RX-	In	Differential twisted pair receive (-), signal line shared with CON2 (pin 6)
7	-	-	75Ω terminal, signal line shared with CON2 (pins 7, 8)
8	LINK_LED	-	Link indicator (low: link established, high: no link)
9	+3.3V_CPU	Power	Power (+3.3V_CPU)[a]
10	GND	Power	Power (GND)

[a]The combined maximum output current of CON1, CON4, CON7 and CON10 is 200mA.

As CON2 and CON7 share the same signal lines they cannot both be used at the same time. Please be sure to use only one of the connectors.

5.3.3. CON3, CON4 (Serial Interface 1) - Armadillo-420/440

CON3 and CON4 are an asynchronous serial interface connected to a UART controller in the i.MX257.

Although CON3 and CON4 have differing connector types and pin layouts, they share the same serial signal lines.

CON3, CON4:

- Signal input/output levels: RS232C levels
- Max data rate: 230.4kbps

- Flow control: CTS, RTS, DTR, DSR, DCD, RI
- Controller: i.MX257 internal UART controller (UART2)
- CON3 connector type: D-Sub 9 pin
- CON4 connector type: 10 pin (2x5, 2.54mm pitch)

The RS232C level conversion IC connected to CON3 and CON4 can be shut down by using the BOOT_MODE1 (GPIO4_31) pin on i.MX257. After the BOOT_MODE1 (GPIO4_31) pin on i.MX257 is set to GPIO output mode, a low signal will activate shut-down mode and a high signal will return the IC to normal mode.

Table 5.9. CON3 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	DCD2	In	Carrier Detect, connected to the UART1_RTS pin on i.MX257, signal line shared with CON4 (pin 1)
2	RXD2	In	Receive Data, connected to the UART2_RXD pin on i.MX257, signal line shared with CON4 (pin 3)
3	TXD2	Out	Transmit Data, connected to UART2_TXD pin on i.MX257, signal line shared with CON4 (pin 5)
4	DTR2	Out	Data Terminal Ready, connected to UART1_RXD on i.MX257, signal line shared with CON4 (pin 7)
5	GND	Power	Power (GND)
6	DSR2	In	Data Set Ready, connected to UART1_TXD pin on i.MX257, signal line shared with CON4 (pin 2)
7	RTS2	Out	Request To Send, connected to UART2_CTS pin on i.MX257, signal line shared with CON4 (pin 4)
8	CTS2	In	Clear To Send, connected to UART2_RTS pin on i.MX257, signal line shared with CON4 (pin 6)
9	RI2	In	Ring Indicator, connected to UART1_CTS pin on i.MX257, signal line shared with CON4 (pin 8)

Table 5.10. CON4 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	DCD2	In	Carrier Detect, connected to the UART1_RTS pin on i.MX257, signal line shared with CON3 (pin 1)
2	DSR2	In	Data Set Ready, connected to UART1_TXD pin on i.MX257, signal line shared with CON3 (pin 6)
3	RXD2	In	Receive Data, connected to the UART2_RXD pin on i.MX257, signal line shared with CON3 (pin 2)
4	RTS2	Out	Request To Send, connected to UART2_CTS pin on i.MX257, signal line shared with CON3 (pin 7)
5	TXD2	Out	Transmit Data, connected to UART2_TXD pin on i.MX257, signal line shared with CON3 (pin 3)
6	CTS2	In	Clear To Send, connected to UART2_RTS pin on i.MX257, signal line shared with CON3 (pin 8)
7	DTR2	Out	Data Terminal Ready, connected to UART1_RXD on i.MX257, signal line shared with CON3 (pin 4)
8	RI2	In	Ring Indicator, connected to UART1_CTS pin on i.MX257, signal line shared with CON3 (pin 9)
9	GND	Power	Power (GND)
10	+3.3V_CPU /+3.3V_EXT	Power	Power (+3.3V_CPU)[a]

[a]The combined maximum output current of CON1, CON4, CON7 and CON10 on Armadillo-420/440 is 200mA.

As CON3 and CON4 share the same signal lines they cannot both be used at the same time. Please be sure to use only one of the connectors.

5.3.4. CON5, CON6 (USB Interface) - Armadillo-420/440

CON5 is a USB interface connected to the USB controller on i.MX257. The USB interface includes two interfaces: USB Interface 1 and USB Interface 2. The USB interface specifications are shown in Table 5.11, “USB Interface - Armadillo-420/440”.

Table 5.11. USB Interface - Armadillo-420/440

USB interface	Connector	Data Transmission Mode	Controller	PHY
USB Interface 1	CON5 (lower) CON6[a]	USB 2.0 High Speed (480Mbps) Full Speed (12Mbps) Low Speed (1.5Mbps)	OTG[b]	USBPHY1[c]
USB Interface 2	CON5 (upper)	USB 2.0 Full Speed (12Mbps) Low Speed (1.5Mbps)	HOST[b]	USBPHY2[c]

[a] Although the lower port of CON5 and CON6 have differing connector types and pin layouts, they share the same USB signal lines.

[b] i.MX257 internal USB controller

[c] i.MX257 internal USB PHY

It is possible to select between the power in VIN of CON12 (or CON13) and the +5V power generated by the power management IC (PMIC) as the source of power provided to USB devices from the USB interface on Armadillo-420/440. The NFWE_B (GPIO3_26) pin on the i.MX257 is used for the power source selection. Power in VIN is used when the NFWE_B (GPIO3_26) pin is low and the PMIC generated +5V is used when it is high. Please refer to Section 3.2.2, “Power Circuit Make-up - Armadillo-420/440” for more details.

The transmission speed shown in brackets under the data transmission mode is the theoretical maximum of the specification. Please be sure to fully check that the actual transmission speed meets any system requirements.

When using USB devices and a power input of less than 4.75V, please use the PMIC generated +5V power supply.

Please be aware that the total maximum current that can be supplied to the two USB channels is 300mA when using the PMIC generated +5V power source.

Table 5.12. CON5 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	+5V_USB	Power	USB power (Warning), max 500mA supply possible when power in VIN (greater than 4.75V) selected.
2	USB1-	In/Out	USB1 minus side signal, i.MX257 USBPHY1_DM pin connection, signal line shared with CON6 (pin 2)

Pin Number	Signal Name	I/O	Function
3	USB1+	In/Out	USB1 plus side signal, i.MX257 USBPHY1_DP pin connection, signal line shared with CON6 (pin 3)
4	GND	Power	Power (GND)
5	+5V_USB	Power	USB power (Warning), max 500mA supply possible when power in VIN (greater than 4.75V) selected.
6	USB2-	In/Out	USB2 minus side signal,
7	USB2+	In/Out	USB2 plus side connection,
8	GND	Power	Power (GND)

Table 5.13. CON6 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	+5V_USB	Power	USB power (Warning), max 500mA supply possible when power in VIN (greater than 4.75V) selected.
2	USB1-	In/Out	USB1 minus side signal, i.MX257 USBPHY1_DM pin connection, signal line shared with CON5 (pin 2)
3	USB1+	In/Out	USB1 plus side signal, i.MX257 USBPHY1_DP pin connection, signal line shared with CON5 (pin 3)
4	GND	Power	Power (GND)

As CON6 and the lower port on CON5 share the same signal lines they cannot both be used at the same time. Please be sure to use only one of the connectors.

When using the +5V produced by the PMIC for the USB power supply (+5V_USB), please use within the range of VIN=DC3.1 - 4.8V. Please note that when VIN > 4.8V, the booster circuit of the PMIC may not function properly and the USB power supply may not meet the required standard value of +5V±5%. When using VIN > 4.8V, please use VIN instead of the +5V from the PMIC for the USB power supply.

Information on tested USB devices is available on the Armadillo Site and is updated regularly.

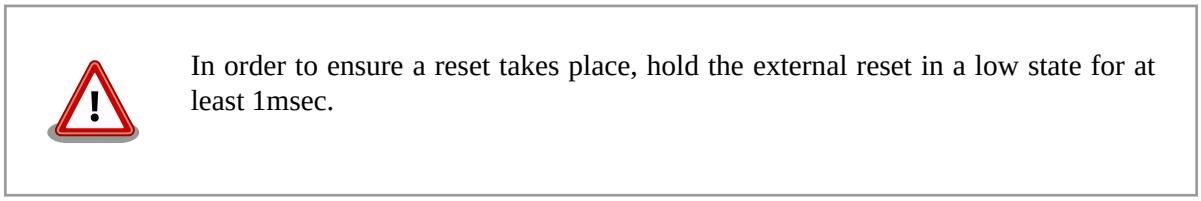
5.3.5. CON8 (External Reset) - Armadillo-420/440

CON8 is an external reset terminal. CON8 (pin 1) is connected to the reset IC incorporated on the board, and while this signal is low the board will be placed in a reset state.

Table 5.14. CON8 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	EXT_RESET*	In	External Reset (low: reset state, high[a]: no reset)
2	GND	Power	Power (GND)

[a] Pin 1 on CON8 is internally pulled up to +3.3V and can accept input from other open collector or open drain signals.



In order to ensure a reset takes place, hold the external reset in a low state for at least 1msec.

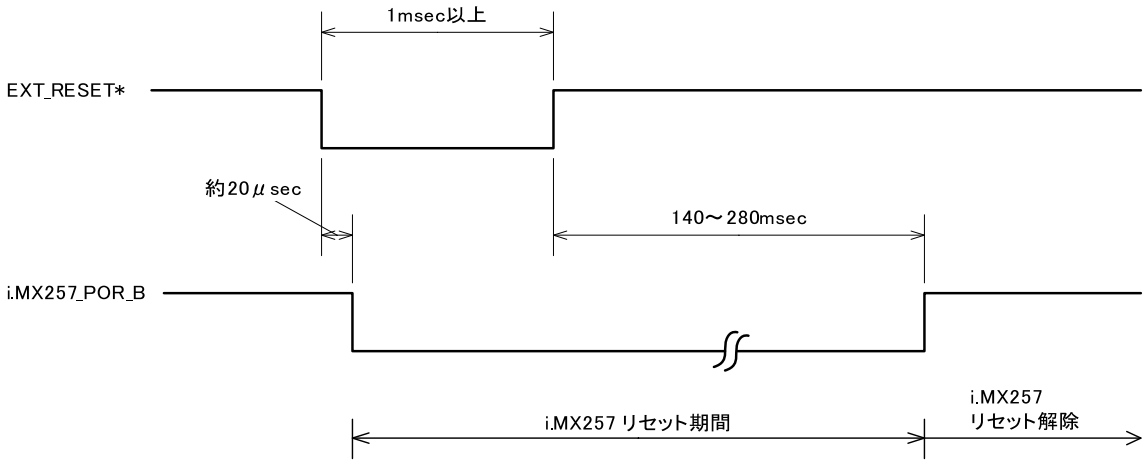


Figure 5.4. EXT_RESET* Timing Chart - Armadillo-420/440

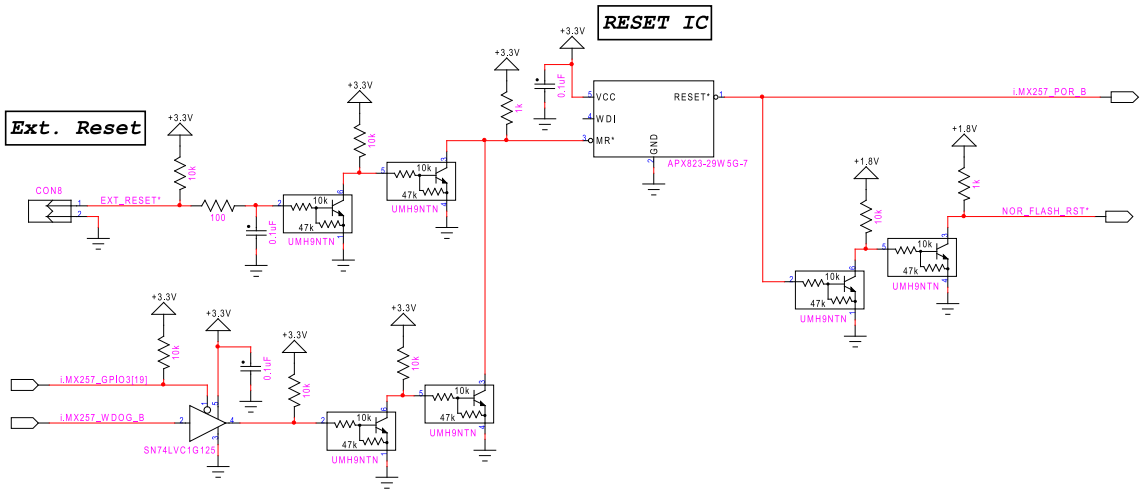


Figure 5.5. EXT_RESET* Circuit Make-up - Armadillo-420/440

5.3.6. CON9 Expansion Interface 1 - Armadillo-420/440

CON9 is an expansion input/output interface. The signal layout is the same throughout the Armadillo-400 Series. Multiple functions are assigned to a single pin on Expansion Interface 1 so that many different functions can be selected depending on the intended use. This is called multiplexing. For a description of the pin signals please refer to Table 5.15, “CON9 Signals - Armadillo-420/440”, for the multiplexed functions please refer to Table 5.16, “CON9 Signal Multiplex - Armadillo-420/440”, and for the initial state of each signal pin please refer to Appendix B, Initial Configuration State of Expansion Interfaces.

The signal layouts of CON8, CON9 and CON14 are the same throughout the Armadillo-400 Series, and the Armadillo-400 Series option modules can be used with either of Armadillo-420/440/460.

Table 5.15. CON9 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	EXT_IO0	In/Out	Expansion I/O 0, connected to VSTBY_REQ pin on i.MX257
2	EXT_IO1	In/Out	Expansion I/O 1, connected to RTCK pin on i.MX257
3	EXT_IO2	In/Out	Expansion I/O 2, connected to CSPI1_MOSI pin on i.MX257
4	EXT_IO3	In/Out	Expansion I/O 3, connected to CSI_D2 pin on i.MX257
5	EXT_IO4	In/Out	Expansion I/O 4, connected to CSPI1_MISO pin on i.MX257
6	EXT_IO5	In/Out	Expansion I/O 5, connected to CSI_D3 pin on i.MX257
7	+3.3V_IO	Power	Power (+3.3V_IO)
8	+3.3V_IO	Power	Power (+3.3V_IO)
9	GND	Power	Power (GND)
10	GND	Power	Power (GND)
11	EXT_IO6	In/Out	Expansion I/O 6, connected to CSPI1_SS1 pin on i.MX257
12	EXT_IO7	In/Out	Expansion I/O 7, connected to CSI_D4 pin on i.MX257
13	EXT_IO8	In/Out	Expansion I/O 8, connected to CSPI1_SCLK pin on i.MX257
14	EXT_IO9	In/Out	Expansion I/O 9, connected to CSI_D5 pin on i.MX257
15	EXT_IO10	In/Out	Expansion I/O 10, connected to CSI_D8 pin on i.MX257
16	EXT_IO11	In/Out	Expansion I/O 11, connected to CSI_D6 pin on i.MX257
17	EXT_IO12	In/Out	Expansion I/O 12, connected to CSI_D9 pin on i.MX257
18	EXT_IO13	In/Out	Expansion I/O 13, connected to CSI_D7 pin on i.MX257
19	GND	Power	Power (GND)
20	+3.3V_IO	Power	Power (+3.3V_IO)
21	EXT_IO14	In/Out	Expansion I/O 14, connected to CSI_MCLK pin on i.MX257
22	EXT_IO15	In/Out	Expansion I/O 15, connected to CSI_VSYNC pin on i.MX257
23	EXT_IO16	In/Out	Expansion I/O 16, connected to CSI_HSYNC pin on i.MX257
24	EXT_IO17	In/Out	Expansion I/O 17, connected to CSI_PIXCLK pin on i.MX257
25	EXT_IO18	In/Out	Expansion I/O 18, connected to CSPI1_SS0 pin on i.MX257
26	EXT_IO19	In/Out	Expansion I/O 19, connected to CSPI1_RDY pin on i.MX257
27	EXT_IO20	In/Out	Expansion I/O 20, connected to CLKO pin on i.MX257
28	EXT_IO21	In/Out	Expansion I/O 21, connected to EXT_ARMCLK pin on i.MX257

Table 5.16. CON9 Signal Multiplex - Armadillo-420/440

Pin Number	Function[a][b]										
	GPIO	CSPI1	CSPI3	UART3	UART5	SD2	CSI	AUD6	SIM1[c]	SIM2[c]	Other
1	GPIO3_17										
2	GPIO3_14										1-WIRE
3	GPIO1_14	MOSI		RXD							
4	GPIO1_27		MOSI		RXD	DAT4	D2		CLK0		
5	GPIO1_15	MISO		TXD							
6	GPIO1_28		MISO		TXD	DAT5	D3		RST0		
7											
8											
9											
10											
11	GPIO1_17	SS1		RTS							
12	GPIO1_29		SCLK		RTS	DAT6	D4		VEN0		
13	GPIO1_18	SCLK		CTS							
14	GPIO1_30		RDY		CTS	DAT7	D5		TX0		
15	GPIO1_7		SS2				D8	RXC		CLK0	
16	GPIO1_31		SS0			CMD	D6		PD0		
17	GPIO4_21		SS3				D9	RXFS		RST0	
18	GPIO1_6		SS1			CLK	D7		RX0		
19											
20											
21	GPIO1_8					DAT0	MCLK	TXD		VEN0	
22	GPIO1_9					DAT1	VSYNC	RXD		TX0	
23	GPIO1_10					DAT2	HSYNC	TXC		PD0	
24	GPIO1_11					DAT3	PIXCLK	TXFS		RX0	
25	GPIO1_16	SS0									PWMO2
26	GPIO2_22	RDY									
27	GPIO2_21										CLKO
28	GPIO3_15										

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

[c]As the SIM function has not be verified, there is no guarantee of its operation.

5.3.7. CON10 (i.MX257 JTAG Interface) - Armadillo-420/440

CON10 is an interface for connecting JTAG debuggers. It is connected to the JTAG Controller in the i.MX257.

It is possible to convert this interface to the standard ARM 20 pin layout with the Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00) option. For details, please see Appendix A, Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00).

Table 5.17. CON10 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	+3.3V_CPU	Power	Power (+3.3V_CPU)
2	JTAG_TRST*	In	Test Reset, connected to TRSTB pin on i.MX257
3	JTAG_TDI	In	Test Data In, connected to TDI pin on i.MX257
4	JTAG_TMS	In	Test Mode Select, connected to TMS pin on i.MX257
5	JTAG_TCK	In	Test Clock, connected to TCK pin on i.MX257
6	JTAG_TDO	Out	Test Data Out, connected to TDO pin on i.MX257
7	CPU_RESET*	In	i.MX257 reset[a], connected to RESET_B pin on i.MX257
8	GND	Power	Power (GND)

[a] Only i.MX257 is reset with the CPU_RESET* pin. If a full board reset is required, please use the EXT_RESET* pin on CON8.

The combined maximum output current of CON1, CON4, CON7 and CON10 on Armadillo-420/440 is 200mA.

5.3.8. CON11 (LCD Expansion Interface) - Armadillo-440

CON11 is a LCD expansion interface which connects to LCD modules with digital RGB inputs. It has connections to a number of functions in the i.MX257, including the LCD controller and touch screen controller. For the signal pin layout please refer to Table 5.18, “CON11 Signals - Armadillo-440”, and for the initial state of each signal pin, please refer to Appendix B, Initial Configuration State of Expansion Interfaces.

The signal layout of CON11 is the same on Armadillo-440 and Armadillo-460, and the Armadillo-400 Series LCD Expansion Board can be used with both Armadillo-440 and Armadillo-460.

Also, as CON11 is multiplexed many different functions can be selected. For information on the multiplexed functions, please refer to Table 5.19, “CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-420/440” and Table 5.20, “CON11 Signal Multiplexing (pins 39 - 50)”.

- Max resolution: 800x600 (18bit)
- Supported touch screens: 4-Wire Resistive
- Connector Type: 50 pin FFC connector (0.5mm pitch)

Table 5.18. CON11 Signals - Armadillo-440

Pin Number	Signal Name	I/O	Function
1	VIN	Power	Power (CON12 or CON13 power in)
2	VIN	Power	Power (CON12 or CON13 power in)
3	VIN	Power	Power (CON12 or CON13 power in)
4	+3.3V_IO	Power	Power (+3.3V_IO)
5	+3.3V_IO	Power	Power (+3.3V_IO)
6	GND	Power	Power (GND)
7	GND	Power	Power (GND)
8	LCD_LSCLK	Out	Connected to LSCLK pin on i.MX257
9	LCD_HSYN	Out	Connected to HSYNC pin on i.MX257
10	LCD_VSYN	Out	Connected to VSYNC pin on i.MX257
11	LCD_OE_ACD	Out	Connected to OE_ACD pin on i.MX257
12	PWMO1	Out	Connected to PWM pin on i.MX257
13	LCD_LD0	Out	Connected to LD0 pin on i.MX257
14	LCD_LD1	Out	Connected to LD1 pin on i.MX257
15	LCD_LD2	Out	Connected to LD2 pin on i.MX257
16	LCD_LD3	Out	Connected to LD3 pin on i.MX257
17	LCD_LD4	Out	Connected to LD4 pin on i.MX257
18	LCD_LD5	Out	Connected to LD5 pin on i.MX257
19	GND	Power	Power (GND)
20	LCD_LD6	Out	Connected to LD6 pin on i.MX257
21	LCD_LD7	Out	Connected to LD7 pin on i.MX257
22	LCD_LD8	Out	Connected to LD8 pin on i.MX257
23	LCD_LD9	Out	Connected to LD9 pin on i.MX257
24	LCD_LD10	Out	Connected to LD10 pin on i.MX257
25	LCD_LD11	Out	Connected to LD11 pin on i.MX257
26	GND	Power	Power (GND)
27	LCD_LD12	Out	Connected to LD12 pin on i.MX257
28	LCD_LD13	Out	Connected to LD13 pin on i.MX257
29	LCD_LD14	Out	Connected to LD14 pin on i.MX257
30	LCD_LD15	Out	Connected to LD15 pin on i.MX257
31	LCD_LD16	Out	Connected to GPIO_E pin on i.MX257
32	LCD_LD17	Out	Connected to GPIO_F pin on i.MX257
33	GND	Power	Power (GND)
34	TOUCH_XP	In/Out	Connected to XP pin on i.MX257
35	TOUCH_XN	In/Out	Connected to XN pin on i.MX257
36	TOUCH_YP	In/Out	Connected to YP pin on i.MX257
37	TOUCH_YN	In/Out	Connected to YN pin on i.MX257
38	GND	Power	Power (GND)
39	EXT_IO24	In/Out	Expansion I/O 24, connected to DE_B pin on i.MX257
40	EXT_IO25	In/Out	Expansion I/O 25, connected to KPP_ROW0 pin on i.MX257
41	EXT_IO26	In/Out	Expansion I/O 26, connected to KPP_ROW1 pin on i.MX257
42	EXT_IO27	In/Out	Expansion I/O 27, connected to KPP_ROW2 pin on i.MX257
43	EXT_IO28	In/Out	Expansion I/O 28, connected to KPP_ROW3 pin on i.MX257
44	EXT_IO29	In/Out	Expansion I/O 29, connected to KPP_COL0 pin on i.MX257
45	EXT_IO30	In/Out	Expansion I/O 30, connected to KPP_COL1 pin on i.MX257
46	EXT_IO31	In/Out	Expansion I/O 31, connected to KPP_COL2 pin on i.MX257
47	EXT_IO32	In/Out	Expansion I/O 32, connected to KPP_COL3 pin on i.MX257
48	EXT_IO33	In/Out	Expansion I/O 33, connected to GPIO_A pin on i.MX257
49	EXT_IO34	In/Out	Expansion I/O 34, connected to GPIO_B pin on i.MX257
50	GND	Power	Power (GND)

Table 5.19. CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-420/440

Pin Number	Function[a][b]					
	LCDC	SLCDC	ADC	SIM1[c]	SIM2[c]	Other
1						
2						
3						
4						
5						
6						
7						
8	LSCLK	CS			PD1	
9	HSYN				VEN1	
10	VSYN				TX1	
11	OE_ACD	RS			RX1	
12						PWMO1
13	LD0	D0		CLK1		
14	LD1	D1		RST1		
15	LD2	D2		VEN1		
16	LD3	D3		TX1		
17	LD4	D4		PD1		
18	LD5	D5		RX1		
19						
20	LD6	D6			CLK1	
21	LD7	D7			RST1	
22	LD8	D8				
23	LD9	D9				
24	LD10	D10				
25	LD11	D11				
26						
27	LD12	D12				
28	LD13	D13				
29	LD14	D14				
30	LD15	D15				
31	LD16					
32	LD17					
33						
34			XP			
35			XN			
36			YP			
37			YN			
38						

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

[c]As the SIM function has not be verified, there is no guarantee of its operation.

Table 5.20. CON11 Signal Multiplexing (pins 39 - 50)

Pin Number	Function[a][b]							
	GPIO	UART3	UART4	AUD5	KPP	I2C3	CAN1	Other
39	GPIO2_20							
40	GPIO2_29	RTD			ROW0			
41	GPIO2_30	TXD			ROW1			
42	GPIO2_31	RTS		RXC	ROW2			
43	GPIO3_0	CTS		RXFS	ROW3			

Pin Number	Function[a][b]							
	GPIO	UART3	UART4	AUD5	KPP	I2C3	CAN1	Other
44	GPIO3_1		RXD	TXD	COL0			
45	GPIO3_2		TXD	RXD	COL1			
46	GPIO3_3		RTS	TXC	COL2			
47	GPIO3_4		CTS	TXFS	COL3			
48	GPIO1_0				ROW4	SCL	TX	PWMO2
49	GPIO1_1				ROW5	SDA	RX	PWMO3
50								

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

5.3.9. CON12, CON13 (Power In) - Armadillo-420/440

CON12 is a DC jack which supplies power to Armadillo-420/440. The AC adapter jack type is EIAJ RC-5320A compliant (voltage classification 2). Jacks with the same polarity mark as Figure 5.6, “AC Adapter Polarity Mark - Armadillo-420/440” can be used.

Figure 5.6. AC Adapter Polarity Mark - Armadillo-420/440

CON13 is a connector which supplies power to the board. Signal lines to control the power management IC (PMIC) on/off are included in this connector.

Table 5.21. CON13 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	GND	Power	Power (GND)
2	VIN	Power	Power in terminal, line shared with center pin of CON12
3	GND	Power	Power (GND)
4	PMIC_ONOFF*	In	PMIC ON/OFF control (2sec or longer GND short to power off, GND short again to power back on)[a]

[a]PMIC_ONOFF* has a 10kΩ pull-up from power in VIN

CON12 and CON13 on Armadillo-420/440 accept a power in voltage range of DC3.1V to 5.25V. Do not apply a voltage higher than 5.25V as this may damage the internal devices.

As the power lines of CON12 and CON13 on Armadillo-420/440 are connected they cannot both be used at the same time. Please be sure to only supply power with one of the connectors.

After the board has been powered off with the PMIC_ONOFF* signal, when disconnecting and then soon reconnecting the power supply to CON12 the PMIC will not power back on and the board will not boot. The board can be booted by shorting the PMIC_ONOFF* signal to GND.

5.3.10. CON14 (Expansion Interface 2) - Armadillo-420/440

CON14 is an expansion input/output interface. Multiple functions are assigned to a single pin so that many different functions can be selected depending on the intended use. For a description of the pin signals please refer to Table 5.23, “CON14 Signal Multiplex - Armadillo-420/440”, for the multiplexed functions please refer to Table 5.23, “CON14 Signal Multiplex - Armadillo-420/440”, and for the initial state of each signal pin please refer to Appendix B, Initial Configuration State of Expansion Interfaces.

The signal layouts of CON8, CON9 and CON14 are the same throughout the Armadillo-400 Series, and the Armadillo-400 Series option modules can be used with either of Armadillo-420/440/460.

Table 5.22. CON14 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	+3.3V_IO	Power	Power (+3.3V_IO)
2	GND	Power	Power (GND)
3	EXT_IO22	In/Out	Expansion I/O 22, connected to GPIO_C pin on i.MX257
4	EXT_IO23	In/Out	Expansion I/O 23, connected to GPIO_D pin on i.MX257

Table 5.23. CON14 Signal Multiplex - Armadillo-420/440

Pin Number	Function[a][b]				
	GPIO	CSPI1	I2C2	CAN2	Other
1					
2					
3	GPIO1_2	SS2	SCL	TX	PWMO4
4	GPIO1_3		SDA	RX	

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

5.3.11. LED1, LED2 (LAN LEDs) - Armadillo-420/440

LED1 and LED2 are the LAN interface status LEDs. They are shown on the upper part of CON2.

Table 5.24. LAN LED Meanings - Armadillo-420/440

LED	Name (color)	On	Off
LED1	Link LED (green)	A LAN cable is connected and a 10BASE-T or 100BASE-TX link has been established.	A LAN cable is not connected or the LAN status of the connected device is not active.
LED2	Activity LED (yellow)	Data transmit/receive	No data

5.3.12. LED3, LED4, LED5 (User LEDs) - Armadillo-420/440

LED3, LED4 and LED5 are LEDs which can be used freely by the user. These LEDs can be controlled once the i.MX257 signals they are connected to are set to GPIO output mode.

Table 5.25. User LED Function - Armadillo-420/440

LED	Name (color)	Function
LED3	User LED (red)	Connected to NFALE (GPIO3_28) pin on i.MX257 (low: off, high: on)

LED	Name (color)	Function
LED4	User LED (green)	Connected to NFCLE (GPIO3_29) pin on i.MX257 (low: off, high: on)
LED5	User LED (yellow)	Connected to BOOT_MODE0 (GPIO4_30) pin on i.MX257 (low: off, high: on)

LED5 is connected to the same signal as JP1. LED5 cannot be controlled while JP1 is shorted.

5.3.13. SW1 (User Switch) - Armadillo-420/440

SW1 is a switch which can be freely used by the user. It is connected to GPIO3_30 on i.MX257. The switch status can be obtained once the i.MX257 signal it is connected to is set to GPIO input mode.

Table 5.26. User Switch Function - Armadillo-420/440

SW	Function
SW1, SW3	Connected to NFWP_B (GPIO3_30) pin on i.MX257 (low: switch pressed, high: switch not pressed)

5.3.14. JP1 (Boot Mode Configuration Jumper) - Armadillo-420/440

The JP1 jumper is used to configure the board's boot mode. The boot mode is determined at power on time according to the jumper state.

Table 5.27. Boot Mode Configuration Jumper States - Armadillo-420/440

JP1	Behavior
Open	On-board flash memory boot
Shorted	UART boot: UART2 (CON3 or CON4)

Table 5.28. JP1 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	JP1	In	Connected to BOOT_MODE0 (GPIO4_30) pin on i.MX257 (10kΩ pull-down)
2	JP1PU	Out	390Ω pull-up by 3.3V_CPU

JP1 is connected to the same signal as LED5. Please do not use JP1 in a shorted state after booting to on-board flash memory.

5.3.15. JP2 (User Jumper) - Armadillo-420/440

The JP2 jumper can be used freely by the user. The jumper status can be obtained once the i.MX257 signal it is connected to is set to GPIO input mode.

Table 5.29. User Jumper Function - Armadillo-420/440

JP	Function
JP2	Connected to NF_CE0 (GPIO3_22) on i.MX257 (low: shorted, high: open)

Table 5.30. JP2 Signals - Armadillo-420/440

Pin Number	Signal Name	I/O	Function
1	GND	Power	Power (GND)
2	JP2	In	Connected to NF_CE0 (GPIO3_22) on i.MX257 (10kΩ pull-up by 3.3V_CPU)

Chapter 6. Interface Specifications - Armadillo-460

6.1. Interface Layout - Armadillo-460

6.1.1. Armadillo-460 Interface Layout

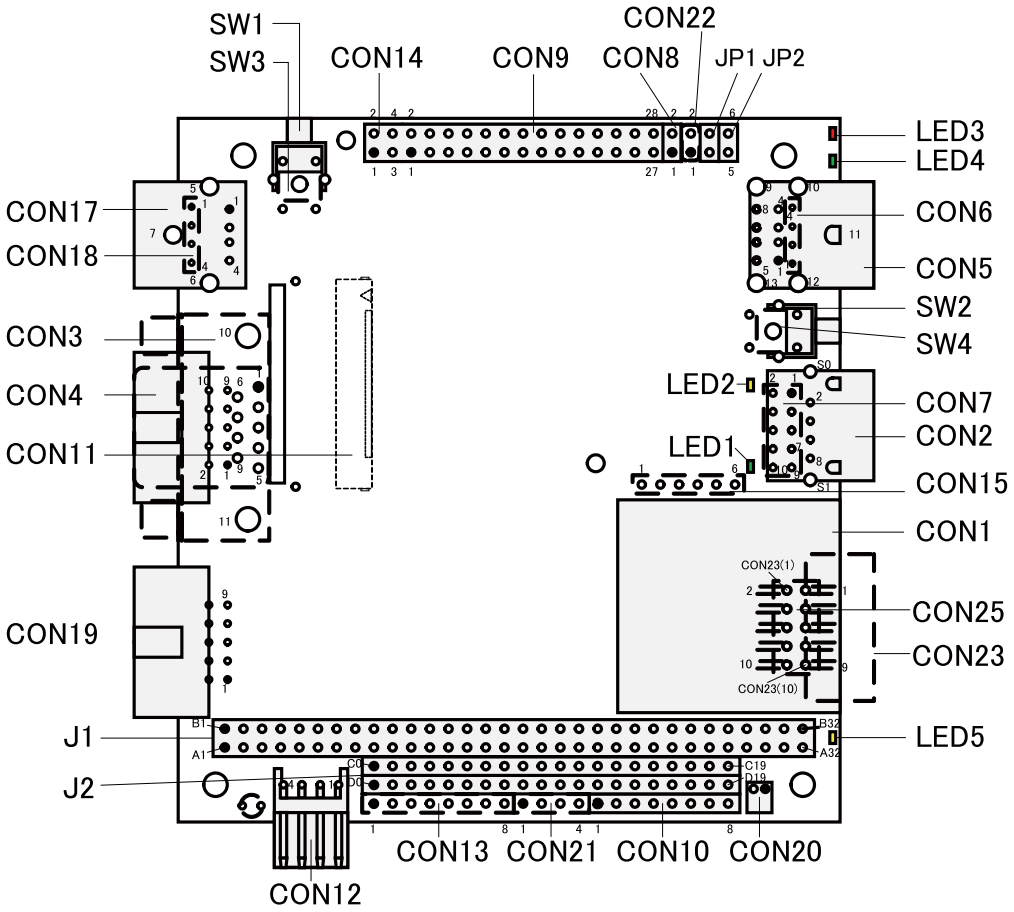


Figure 6.1. Armadillo-460 Interface Layout

Table 6.1. Armadillo-460 Interfaces[a]

Part Number	Interface	Shape	Notes
CON1	SD	SD slot	
CON2	LAN	RJ-45 Connector	
CON3	Serial 1	D-Sub 9 pin (male)	Signal lines shared with CON4
CON4	Serial 1	Pin headers (10P) (2.54mm pitch)	
CON5	USB	Type-A connector (1 port)	High Speed support 2 port stack connector option, support for Full Speed on upper, High Speed on lower

Part Number	Interface	Shape	Notes
CON6	USB	Pin headers (4P) (2.54mm pitch)	Signal lines shared with lower port of CON5
CON7	LAN	Pin headers (10P) (2.54mm pitch)	Some signal lines shared with CON2
CON8	External Reset	Pin headers (2P) (2.54mm pitch)	
CON9	Expansion 1	Pin headers (28P) (2.54mm pitch)	
CON10	i.MX257 JTAG	Pin headers (8P) (2.54mm pitch)	
CON11	LCD Expansion	FFC Connector (50P) (0.5mm pitch)	
CON12	Power in	Pin headers (4P) (2.5mm pitch)	
CON13	Power in	Pin headers (8P) (2.54mm pitch)	
CON14	Expansion 2	Pin headers (4P) (2.54mm pitch)	
CON15	Reserved		
CON17	USB	Type-A connector (1 port)	Full Speed support
CON18	USB	Pin headers (4P) (2.54mm pitch)	Signal lines shared with CON17
CON19	Serial 4	Pin headers (10P) (2.54mm pitch)	
CON20	RTC External Backup Power In	Pin headers (2P) (1.25mm pitch)	
CON21	Power Out	Pin headers (4P) (2.54mm pitch)	
CON22	User switch	Pin headers (6P) (2.54mm pitch)	Signal lines shared with SW1
CON23	SD	Pin headers (10P) (2.54mm pitch)	Signal lines shared with CON1
CON24	Reserve	-	-
CON25	SD	Pin headers (10P) (2.54mm pitch)	Signal lines shared with CON1
J1	Expansion Bus	Stack through (64P) (2.54mm pitch)	
J2	Expansion Bus	Stack through (40P) (2.54mm pitch)	
JP1	Boot mode jumper	Pin headers (2P) (2.54mm pitch)	
JP2	User jumper	Pin headers (2P) (2.54mm pitch)	
LED1	LAN Link LED	LED (green, surface mount)	Shown on upper part of CON2
LED2	LAN Activity LED	LED (yellow, surface mount)	Shown on upper part of CON2
LED3	User LED	LED (red, surface mount)	
LED4	User LED	LED (green, surface mount)	
LED5	User LED	LED (yellow, surface mount)	
SW1	User switch	Tact Switch (l=3.3mm) Right-angle	
SW2	Reset Switch	Tact Switch (l=3.3mm) Right-angle	
SW3	User switch	Tact Switch (h=3.5mm) Straight	Signal lines shared with SW1

Part Number	Interface	Shape	Notes
SW4	Reset Switch	Tact Switch (h=3.5mm) Straight	Signal lines shared with SW2

[a]Parts with a white part number background are equipped as standard. Parts with a gray part number background are not equipped as standard, but can be optionally added.

6.2. Electrical Specifications - Armadillo-460

6.2.1. Input/Output Interface Electrical Specifications - Armadillo-460

The rated absolute maximum of the input/output interface is shown in Table 6.2, “Input/Output Interface Rated Absolute Maximum - Armadillo-460”, the power supply specifications in Table 6.3, “Input/Output Interface Power Electrical Specifications - Armadillo-460”, and the electrical specifications in Table 6.4, “Input/Output Interface Electrical Specifications - Armadillo-460”.

With the Software Pad Control (SW_PAD_CTL) and Drive Voltage Select Group Control (SW_PAD_CTL_GRP_DVS) registers in i.MX257 it is possible to alter the output current (Std, High, Max), slew rate (Slow, Fast), and pull-up/pull-down.

Table 6.2. Input/Output Interface Rated Absolute Maximum - Armadillo-460

Symbol	Parameter	Min	Max	Units
VImax	Input voltage range	–0.5	OVDD+0.3	V

Table 6.3. Input/Output Interface Power Electrical Specifications - Armadillo-460

Symbol	Parameter	Min	Max	Units	Conditions
+3.3V_IO	Power Supply Voltage	0.95 x VDD_IO	1.05 x VDD_IO	V	VDD_IO = +3.3V
	Power Supply Current	-	0.5	A	
+3.3V_EXT	Power Supply Voltage	0.95 x VDD_EXT	1.05 x VDD_EXT	V	VDD_EXT = +3.3V
	Power Supply Current	-	1.0	A	

Table 6.4. Input/Output Interface Electrical Specifications - Armadillo-460

Symbol	Parameter	Min	Max	Units	Conditions
VIH	CMOS High-Level Input Voltage	0.7 x OVDD	OVDD	V	OVDD = +3.3V
VIL	CMOS Low-Level Input Voltage	-0.3	0.3 x OVDD	V	OVDD = +3.3V
VOH	CMOS High-Level Output Voltage	OVDD-0.15	-	V	IOH = -1mA
		0.8 x OVDD	-	V	IOH = Specified Drive
VOL	CMOS Low-Level Output Voltage	-	0.15	V	IOL = 1mA
		-	0.2 x OVDD	V	IOL = Specified Drive
IOH_S	High-Level Output Current, Slow Slew Rate	-2.0	-	mA	VOH = 0.8 x OVDD, Std Drive
		-4.0	-	mA	VOH = 0.8 x OVDD, High Drive
		-8.0	-	mA	VOH = 0.8 x OVDD, Max Drive
IOH_F	High-Level Output Current, Fast Slew Rate	-4.0	-	mA	VOH = 0.8 x OVDD, Std Drive
		-6.0	-	mA	VOH = 0.8 x OVDD, High Drive
		-8.0	-	mA	VOH = 0.8 x OVDD, Max Drive
IOL_S	Low-Level Output Current, Slow Slew Rate	2.0	-	mA	VOL = 0.2 x OVDD, Std Drive
		4.0	-	mA	VOL = 0.2 x OVDD, High Drive
		8.0	-	mA	VOL = 0.2 x OVDD, Max Drive

Symbol	Parameter	Min	Max	Units	Conditions
IOL_F	Low-Level Output Current, Fast Slew Rate	4.0	-	mA	VOH = 0.2 x OVDD, Std Drive
		6.0	-	mA	VOH = 0.2 x OVDD, High Drive
		8.0	-	mA	VOH = 0.2 x OVDD, Max Drive
IIN	Input Current (no PU/PD[a])	-	0.1	µA	VI = 0
		-	0.06	µA	VI = OVDD = +3.3V
	Input Current (22kΩPU)	117	184	µA	VI = 0
		0.0001	0.0001	µA	VI = OVDD = +3.3V
	Input Current (47kΩPU)	54	88	µA	VI = 0
		0.0001	0.0001	µA	VI = OVDD = +3.3V
	Input Current (100kΩPU)	25	42	µA	VI = 0
		0.0001	0.0001	µA	VI = OVDD = +3.3V
	Input Current (100kΩPD)	0.0001	0.0001	µA	VI = 0
		25	42	µA	VI = OVDD = +3.3V
ICC	High-impedance Supply Current	-	1.2	µA	VI = 0
		-	1.2	µA	VI = OVDD = +3.3V

[a]PU=Pull Up, PD=Pull Down

6.2.2. Expansion Bus Interface Electrical Specifications - Armadillo-460

The Expansion Bus Interface has a PC/104 expansion bus compatibility mode and a direct CPU bus mode, with power voltage specifications differing between the two modes.

Table 6.5. Expansion Bus Interface Power Electrical Specifications - Armadillo-460

Expansion Bus Interface	min	max	Units
PC/104 Expansion Bus Compatibility Mode	3.0	5.25	V
Direct CPU Bus Mode	3.0	3.6	V

When using the direct CPU bus mode, be sure to use +3.3V_EXT for the PC/104 expansion bus interface power V_PC104. +3.3V_EXT can be selected by replacing the chip resistor (R270) with 0Ω. Please refer to Appendix D, Resistor Information - Armadillo-460 for the position of the chip resistor to replace.

The rated absolute maximum of the expansion bus interface is shown in Table 6.6, “Expansion Bus Interface Rated Absolute Maximum - Armadillo-460”.

The electrical specifications of the Expansion Bus Interface in PC/104 Expansion Bus Compatibility Mode are shown in Table 6.7, “Expansion Bus Interface Electrical Specifications - PC/104 Expansion Bus Compatibility Mode”, while those for the Direct CPU Bus Mode are shown in Table 6.8, “Expansion Bus Interface Electrical Specifications - Direct CPU Bus Mode”.

Table 6.6. Expansion Bus Interface Rated Absolute Maximum - Armadillo-460

Symbol	Parameter	min	max	Units	Condition
VImax	Input voltage range	-0.5	6.0	V	-
VOmax	Output voltage range	-0.5	V_PC104+0.5	V	-
Iomax	output source or sink current	-	±50	mA	VO = 0 V to V_PC104
ICC, IGND	V_PC104 or GND current	-	±100	mA	[SD0..SD7],[SD8..SD15]

Table 6.7. Expansion Bus Interface Electrical Specifications - PC/104 Expansion Bus Compatibility Mode

Symbol	Parameter	min	max	Units	Condition
VIH	HIGH-level input voltage	2.0	-	V	V_PC104=3.0V to 5.5V
VIL	LOW-level input voltage	-	0.7	V	V_PC104=3.0V to 5.5V
VOH	HIGH-level output voltage	V_PC104-0.5	-	V	IO = -12 mA
VOL	LOW-level output voltage	-	0.4	V	IO = 12 mA
ILI	Input leakage current	-	±5	uA	VI = V_PC104 or GND
IOZ	3-state output OFF-state current	-	±10	uA	VI = VIH or VIL VO = V_PC104 or GND

Table 6.8. Expansion Bus Interface Electrical Specifications - Direct CPU Bus Mode

Symbol	Parameter	min	max	Units	Condition
VIH	HIGH-level input voltage	2.0	-	V	V_PC104=3.0V to 3.6V
VIL	LOW-level input voltage	-	0.7	V	V_PC104=3.0V to 3.6V
VOH	HIGH-level output voltage	V_PC104-0.5	-	V	IO = -12 mA
VOL	LOW-level output voltage	-	0.4	V	IO = 12 mA
ILI	Input leakage current	-	±5	uA	VI = V_PC104 or GND
IOZ	3-state output OFF-state current	-	±10	uA	VI = VIH or VIL VO = V_PC104 or GND

6.3. Interfaces - Armadillo-460

6.3.1. CON1, CON23, CON25 (SD Interface) - Armadillo-460

CON1 on Armadillo-460 is a SD slot. It is connected to the SD/MMC controller (SDHC1) on i.MX257. Although CON23, CON25 and CON1 have differing connector types and pin layouts, they share the same SD signal lines.

Power supplied to the SD interface can be turned on and off with the NFRE_B (GPIO3_27) pin on i.MX257. After the NFRE_B (GPIO3_27) pin on i.MX257 is set to GPIO output mode, power supply will start on a low signal and stop on a high signal.

Table 6.9. CON1 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	SD1_DAT3	In/Out	Data bus (bit 3), connected to SD1_DATA3 pin on i.MX257
2	SD1_CMD	In/Out	Command / Response, connected to SD1_CMD pin on i.MX257
3	VSS	Power	Power (GND)
4	VDD	Power	Power (+3.3V_EXT)[a][b]
5	SD1_CLK	Out	Clock, connected to SD1_CLK pin on i.MX257
6	VSS	Power	Power (GND)
7	SD1_DAT0	In/Out	Data bus (bit 0), connected to SD1_DATA0 pin on i.MX257
8	SD1_DAT1	In/Out	Data bus (bit 1), connected to SD1_DATA1 pin on i.MX257
9	SD1_DAT2	In/Out	Data bus (bit 2), connected to SD1_DATA2 pin on i.MX257
10	SD1_CD*	In	Card detect (low: card inserted, high: card ejected), connected to NFRB (GPIO3_31) pin on i.MX257
12	SD1_WP	In	Write protect detect (Low：writable, High：not writable), connected to BCLK (GPIO4_4) pin on i.MX257

[a]The combined maximum output current of CON1, CON4, CON7, CON19, CON21, CON23 and CON25 is 500mA.

[b]CON1 (SD slot) is hot-pluggable.

Table 6.10. Card Detect, Write Protect Detect Functions - Armadillo-460

SD Card	Write Protect	SD1_CD*	SD1_WP
Inserted	Not writable	Low	High
	Writable		Low
Removed	-	High	High

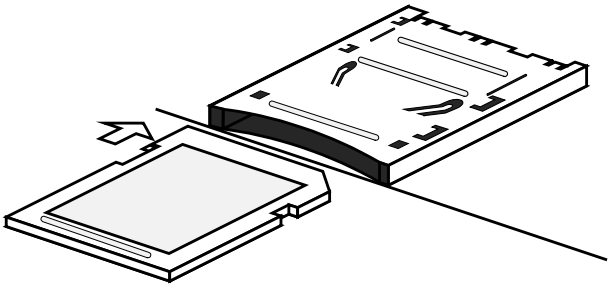


Figure 6.2. SD Card Insertion and Removal - Armadillo-460

As CON1, CON23 and CON25 share the same signal lines they cannot be used at the same time. Please be sure to use only one of the connectors.

Information on tested SD cards is available on the Armadillo Site and is updated regularly.

Table 6.11. CON23 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	SD1_DAT2	In/Out	Data bus (bit 2), connected to SD1_DATA2 pin on i.MX257
2	SD1_DAT3	In/Out	Data bus (bit 3), connected to SD1_DATA3 pin on i.MX257
3	SD1_CMD	In/Out	Command / Response, connected to SD1_CMD pin on i.MX257
4	VSS	Power	Power (GND)
5	VDD	Power	Power (+3.3V_EXT)[a]
6	SD1_CLK	Out	Clock, connected to SD1_CLK pin on i.MX257
7	SD1_DAT0	In/Out	Data bus (bit 0), connected to SD1_DATA0 pin on i.MX257
8	SD1_DAT1	In/Out	Data bus (bit 1), connected to SD1_DATA1 pin on i.MX257
9	SD1_CD*	In	Card detect (low: card inserted, high: card ejected) connected to NFRB (GPIO3_31) pin on i.MX257

Pin Number	Signal Name	I/O	Function
10	SD1_WP	In	Write protect detect (Low：writable, High：not writable), connected to BCLK (GPIO4_4) pin on i.MX257

[a]The combined maximum output current of CON1, CON4, CON7, CON19, CON21, CON23 and CON25 is 500mA.

As CON1, CON23 and CON25 share the same signal lines they cannot be used at the same time. Please be sure to use only one of the connectors.

Please do not apply a voltage greater than 1.8V to the SD1_CD* and SD1_WP signals of CON23 and CON25. Doing so may damage an internal device.

It is not recommended to use the SD1_CD* and SD1_WP signals of CON23 and CON25 as GPIO inputs. If they must be used as GPIO inputs, please connect them as open drain.

Table 6.12. CON25 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	SD1_DAT3	In/Out	Data bus (bit 3), connected to SD1_DATA3 pin on i.MX257
2	SD1_DAT2	In/Out	Data bus (bit 2), connected to SD1_DATA2 pin on i.MX257
3	VSS	Power	Power (GND)
4	SD1_CMD	In/Out	Command / Response, connected to SD1_CMD pin on i.MX257
5	SD1_CLK	Out	Clock, connected to SD1_CLK pin on i.MX257
6	VDD	Power	Power (+3.3V_EXT)[a]
7	SD1_DAT1	In/Out	Data bus (bit 1), connected to SD1_DATA1 pin on i.MX257
8	SD1_DAT0	In/Out	Data bus (bit 0), connected to SD1_DATA0 pin on i.MX257
9	SD1_WP	In	Write protect detect (Low：writable, High：not writable), connected to BCLK (GPIO4_4) pin on i.MX257
10	SD1_CD*	In	Card detect (low: card inserted, high: card ejected) connected to NFRB (GPIO3_31) pin on i.MX257

[a]The combined maximum output current of CON1, CON4, CON7, CON19, CON21, CON23 and CON25 is 500mA.

6.3.2. CON2, CON7 (LAN Interface) - Armadillo-460

CON2 and CON7 are a 10BASE-T/100BASE-TX LAN interface which can be used with Category 5 or above Ethernet cables. The interface includes AUTO-MDIX functionality allowing it to automatically detect straight or cross cable connections and swap the send and receive terminals accordingly.

Table 6.13. CON2 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	TX+	Out	Differential twisted pair transmit (+), signal line shared with CON7 (pin 1)
2	TX-	Out	Differential twisted pair transmit (-), signal line shared with CON7 (pin 4)
3	RX+	In	Differential twisted pair receive (+), signal line shared with CON7 (pin 3)
4	-	-	75Ω terminal after connection with CON2 (pin 5), signal line shared with CON7 (pin 5)
5	-	-	75Ω terminal after connection with CON2 (pin 4), signal line shared with CON7 (pin 5)
6	RX-	In	Differential twisted pair receive (-), signal line shared with CON7 (pin 6)
7	-	-	75Ω terminal after connection with CON2 (pin 8), signal line shared with CON7 (pin 7)
8	-	-	75Ω terminal after connection with CON2 (pin 7), signal line shared with CON7 (pin 7)

Table 6.14. CON7 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	TX+	Out	Differential twisted pair transmit (+), signal line shared with CON2 (pin 1)
2	ACTIVITY_LED	Out	Activity indicator (low: data transmit/receive, high: no data)
3	RX+	In	Differential twisted pair receive (+), signal line shared with CON2 (pin 3)
4	TX-	Out	Differential twisted pair transmit (-), signal shared with CON2 (pin 2)
5	-	-	75Ω terminal, signal line shared with CON2 (pins 4, 5)
6	RX-	In	Differential twisted pair receive (-), signal line shared with CON2 (pin 6)
7	-	-	75Ω terminal, signal line shared with CON2 (pins 7, 8)
8	LINK_LED	-	Link indicator (low: link established, high: no link)
9	+3.3V_CPU	Power	Power (+3.3V_CPU)[a]
10	GND	Power	Power (GND)

[a]The combined maximum output current of CON1, CON4, CON7 and CON10 is 200mA.

As CON2 and CON7 share the same signal lines they cannot both be used at the same time. Please be sure to use only one of the connectors.

6.3.3. CON3, CON4, CON19 (Serial Interface) - Armadillo-460

CON3, CON4 and CON19 are asynchronous serial interfaces. Serial Interface 1 of CON3 and CON4 is connected to a UART controller in the i.MX257.

Although CON3 and CON4 have differing connector types and pin layouts, they share the same serial signal lines.

Serial Interface 4 of CON19 is connected to a UART controller in the i.MX257 via a selector on Armadillo-460.

6.3.3.1. CON3, CON4 (Serial Interface 1) - Armadillo-460

CON3, CON4:

- Signal input/output levels: RS232C levels
- Max data rate: 230.4kbps
- Flow control: CTS, RTS, DTR, DSR, DCD, RI

- Controller: i.MX257 internal UART controller (UART2)
- CON3 connector type: D-Sub 9 pin
- CON4 connector type: 10 pin (2x5, 2.54mm pitch)

The RS232C level conversion IC connected to CON3 and CON4 can be shut down by using the BOOT_MODE1 (GPIO4_31) pin on i.MX257. After the BOOT_MODE1 (GPIO4_31) pin on i.MX257 is set to GPIO output mode, a low signal will activate shut-down mode and a high signal will return the IC to normal mode.

Table 6.15. CON3 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	DCD2	In	Carrier Detect, connected to the UART1_RTS pin on i.MX257, signal line shared with CON4 (pin 1)
2	RXD2	In	Receive Data, connected to the UART2_RXD pin on i.MX257, signal line shared with CON4 (pin 3)
3	TXD2	Out	Transmit Data, connected to UART2_TXD pin on i.MX257, signal line shared with CON4 (pin 5)
4	DTR2	Out	Data Terminal Ready, connected to UART1_RXD on i.MX257, signal line shared with CON4 (pin 7)
5	GND	Power	Power (GND)
6	DSR2	In	Data Set Ready, connected to UART1_TXD pin on i.MX257, signal line shared with CON4 (pin 2)
7	RTS2	Out	Request To Send, connected to UART2_CTS pin on i.MX257, signal line shared with CON4 (pin 4)
8	CTS2	In	Clear To Send, connected to UART2_RTS pin on i.MX257, signal line shared with CON4 (pin 6)
9	RI2	In	Ring Indicator, connected to UART1_CTS pin on i.MX257, signal line shared with CON4 (pin 8)

Table 6.16. CON4 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	DCD2	In	Carrier Detect, connected to the UART1_RTS pin on i.MX257, signal line shared with CON3 (pin 1)
2	DSR2	In	Data Set Ready, connected to UART1_TXD pin on i.MX257, signal line shared with CON3 (pin 6)
3	RXD2	In	Receive Data, connected to the UART2_RXD pin on i.MX257, signal line shared with CON3 (pin 2)
4	RTS2	Out	Request To Send, connected to UART2_CTS pin on i.MX257, signal line shared with CON3 (pin 7)
5	TXD2	Out	Transmit Data, connected to UART2_TXD pin on i.MX257, signal line shared with CON3 (pin 3)
6	CTS2	In	Clear To Send, connected to UART2_RTS pin on i.MX257, signal line shared with CON3 (pin 8)
7	DTR2	Out	Data Terminal Ready, connected to UART1_RXD on i.MX257, signal line shared with CON3 (pin 4)
8	RI2	In	Ring Indicator, connected to UART1_CTS pin on i.MX257, signal line shared with CON3 (pin 9)
9	GND	Power	Power (GND)
10	+3.3V_EXT	Power	Power (+3.3V_EXT)[a]

[a]The combined maximum output current of CON1, CON4, CON7, CON19, CON21, CON23 and CON25 on Armadillo-460 is 500mA.

As CON3 and CON4 share the same signal lines they cannot both be used at the same time. Please be sure to use only one of the connectors.

6.3.3.2. CON19 (Serial Interface 4) - Armadillo-460

CON19:

- Signal input/output levels: RS232C levels
- Max data rate: 230.4kbps
- Flow control: CTS, RTS
- Controller: i.MX257 internal UART controller (UART4)
- CON19 connector type: 10 pin (2x5, 2.54mm pitch)

Table 6.17. CON19 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	-	-	-
2	-	-	-
3	RXD4	In	Receive Data, connected via a selector to the UART4_RXD pin on i.MX257, selectable exclusively of CON11 (pin 44: AUD5_TXD)
4	RTS4	Out	Request To Send, connected via a selector to the UART4_CTS pin on i.MX257, selectable exclusively of CON11 (pin 47: AUD5_TXFS)
5	TXD4	Out	Transmit Data, connected via selector to UART4_TXD pin on i.MX257 selectable exclusively of CON11 (pin 45: AUD5_RXD)
6	CTS4	In	Clear To Send, connected via a selector to the UART4_RTS pin on i.MX257, selectable exclusively of CON11 (pin 46: AUD5_TXC)
7	-	-	-
8	-	-	-
9	GND	Power	Power (GND)
10	+3.3V_EXT	Power	Power (+3.3V_EXT)[a]

[a]The combined maximum output current of CON1, CON4, CON7, CON19, CON21, CON23 and CON25 on Armadillo-460 is 500mA.

6.3.3.2.1. CON11/CON19 Connection Selector Makeup - Armadillo-460

Details on the CON11/CON19 connection selector on Armadillo-460 are shown in Figure 6.3, “CON11/CON19 Connection Selector - Armadillo-460”. The CON11/CON19 connection selector is used to connect the KPP_COL0/GPIO3_1 pin, KPP_COL1/GPIO3_2 pin, KPP_COL2/GPIO3_3 pin and KPP_COL3/GPIO3_4 pin on i.MX257 to either CON19 or CON11 and is controlled with the Ext I/F Control Register in the CPLD. Please refer to Appendix E, CPLD Registers - Armadillo-460 for details on the CPLD memory map and its registers. For details on the i.MX257 multiplexing, please refer to Table 6.30, “CON11 Signal Multiplexing (pins 39 - 50) - Armadillo-460”.

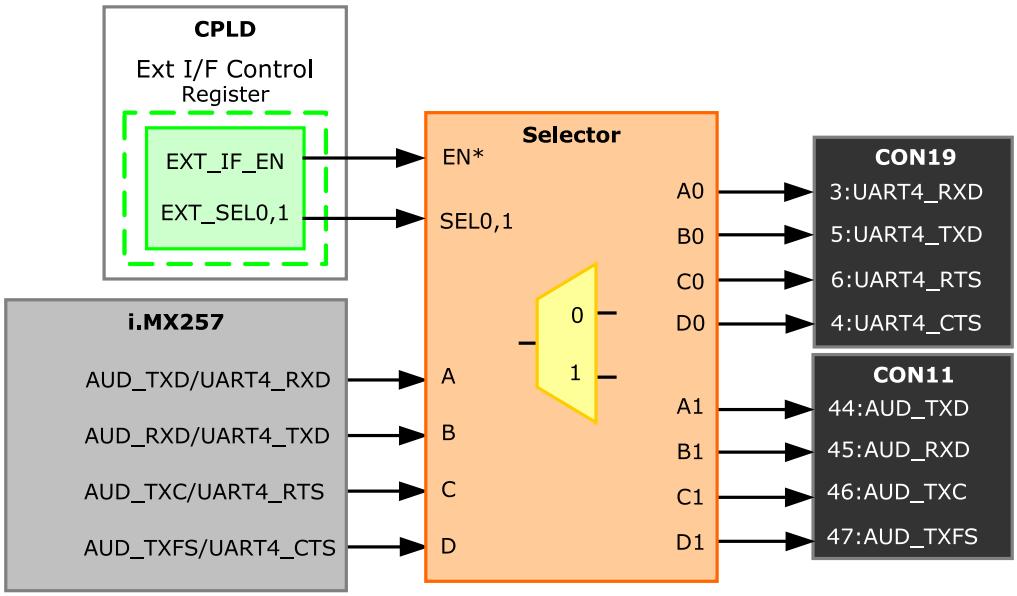


Figure 6.3. CON11/CON19 Connection Selector - Armadillo-460

6.3.4. CON5, CON6, CON17, CON18 (USB Interface) - Armadillo-460

CON5 is a USB interface connected to the USB controller on i.MX257.

The USB interface includes two interfaces: USB Interface 1 and USB Interface 2. The USB interface specifications are shown in Table 6.18, “USB Interface - Armadillo-460”.

Although the lower port of CON5 and CON6 have differing connector types and pin layouts, they share the same USB signal lines.

Although CON17 and the upper port of CON5 have differing connector types and pin layouts, they share the same USB signal lines.

Table 6.18. USB Interface - Armadillo-460

USB interface	Connector	Data Transmission Mode	Controller	PHY
USB Interface 1	CON5 (lower) CON6	USB 2.0 High Speed (480Mbps) Full Speed (12Mbps) Low Speed (1.5Mbps)	OTG[a]	USBPHY1[b]
USB Interface 2	CON5 (upper) CON17 CON18	USB 2.0 Full Speed (12Mbps) Low Speed (1.5Mbps)	HOST[a]	USBPHY2[b]

[a] i.MX257 internal USB controller

[b] i.MX257 internal USB PHY

The transmission speed shown in brackets under the data transmission mode is the theoretical maximum of the specification. Please be sure to fully check that the actual transmission speed meets any system requirements.

On Armadillo-460, the USB Full Speed signals can be output to either CON5 (upper port), CON17 or CON18.

Table 6.19. CON5 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	+5V_USB	Power	Selection between USB power and power in VIN (when above 4.75V) providing for a max 500mA supply
2	USB1-	In/Out	USB1 minus side signal, i.MX257 USBPHY1_DM pin connection, signal line shared with CON6 (pin 2)
3	USB1+	In/Out	USB1 plus side signal, i.MX257 USBPHY1_DP pin connection, signal line shared with CON6 (pin 3)
4	GND	Power	Power (GND)
5	+5V_USB	Power	Selection between USB power and power in VIN (when above 4.75V) providing for a max 500mA supply
6	USB2-	In/Out	USB2 minus side signal, connected to i.MX257 USBPHY2_DM pin, shared with CON17 (pin 2) and CON18 (pin 2)
7	USB2+	In/Out	USB2 plus side connection, connected to i.MX257 USBPHY2_DP pin, shared with CON17 (pin 3) and CON18 (pin 3)
8	GND	Power	Power (GND)

Table 6.20. CON6 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	+5V_USB	Power	Selection between USB power and power in VIN (when above 4.75V) providing for a max 500mA supply
2	USB1-	In/Out	USB1 minus side signal, i.MX257 USBPHY1_DM pin connection, signal line shared with CON5 (pin 2)
3	USB1+	In/Out	USB1 plus side signal, i.MX257 USBPHY1_DP pin connection, signal line shared with CON5 (pin 3)
4	GND	Power	Power (GND)

Table 6.21. CON17 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	+5V_USB	Power	Selection between USB power and power in VIN (when above 4.75V) providing for a max 500mA supply
2	USB2-	In/Out	USB2 minus side signal, connected to i.MX257 USBPHY2_DM pin, shared with CON5 (pin 6) and CON18 (pin 3)
3	USB2+	In/Out	USB2 plus side connection, connected to i.MX257 USBPHY2_DP pin, shared with CON5 (pin 7) and CON18 (pin 3)
4	GND	Power	Power (GND)

Table 6.22. CON18 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	+5V_USB	Power	Selection between USB power and power in VIN (when above 4.75V) providing for a max 500mA supply
2	USB2-	In/Out	USB2 minus side signal, connected to i.MX257 USBPHY2_DM pin, shared with CON5 (pin 6) and CON17 (pin 2)
3	USB2+	In/Out	USB2 plus side connection, connected to i.MX257 USBPHY2_DP pin, shared with CON5 (pin 7) and CON17 (pin 3)

Pin Number	Signal Name	I/O	Function
4	GND	Power	Power (GND)

As CON6 and the lower port on CON5 share the same signal lines they cannot both be used at the same time. Please be sure to use only one of the connectors.

As CON17, CON18 and the upper port on CON5 share the same signal lines they cannot be used at the same time. Please be sure to use only one of the connectors.

Information on tested USB devices is available on the Armadillo Site and is updated regularly.

6.3.5. CON8, SW2, SW4 (External Reset) - Armadillo-460

CON8 is an external reset terminal. CON8 (pin 1) is connected to the reset IC incorporated on the board, and while this signal is low Armadillo-460 will be placed in a reset state. SW2 and SW4 share the CON8 reset signal.

Table 6.23. CON8 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	EXT_RESET*	In	External Reset (low: reset state, high[a]: no reset)
2	GND	Power	Power (GND)

[a]Pin 1 on CON8 is internally pulled up to +3.3V and can accept input from other open collector or open drain signals.

Table 6.24. Reset Switch Function - Armadillo-460

SW	Function
SW2, SW4	External Reset (pressed: reset state, not pressed[a]: no reset)

[a]Pin 1 on CON8 is internally pulled up to +3.3V and can accept input from other open collector or open drain signals.

In order to ensure a reset takes place, hold the external reset in a low state for at least 1msec.

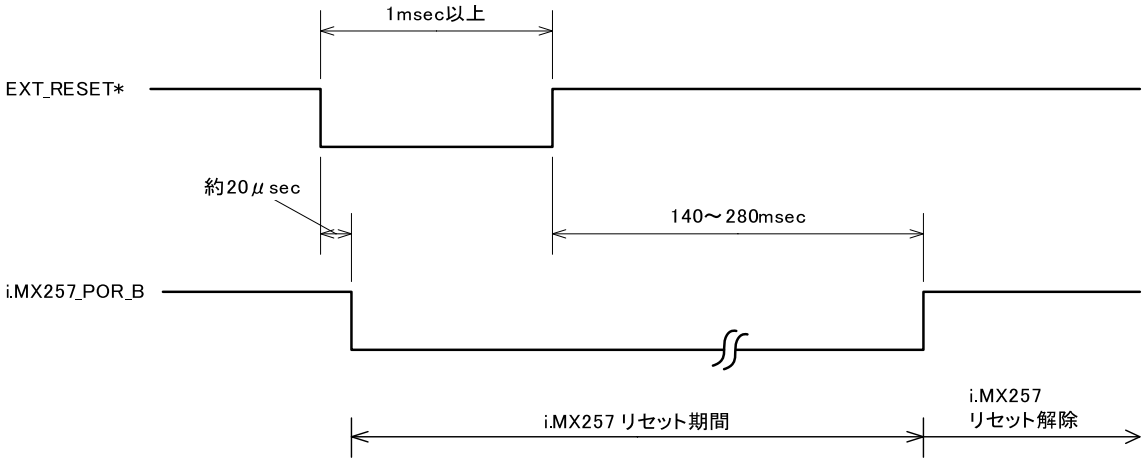


Figure 6.4. EXT_RESET* Timing Chart - Armadillo-460

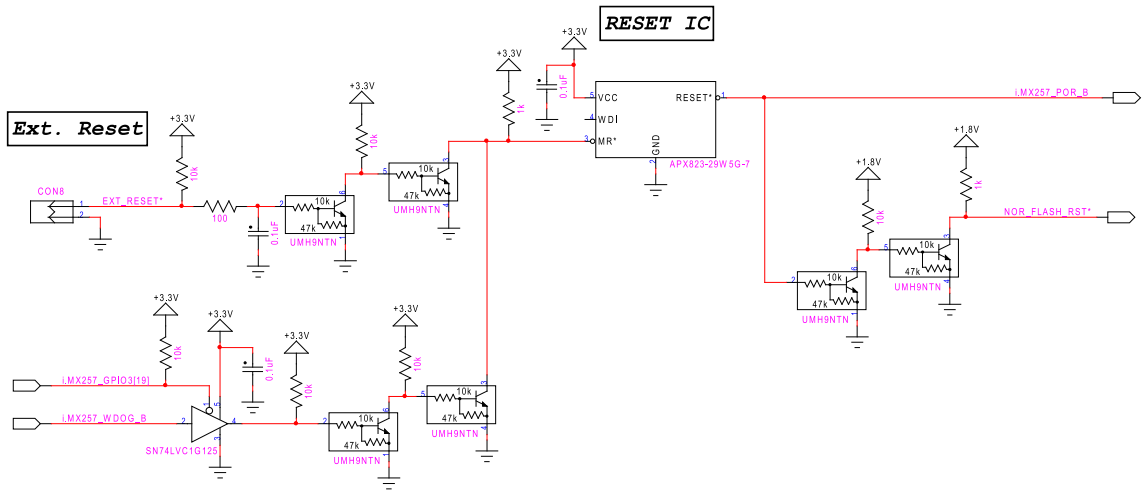


Figure 6.5. EXT_RESET* Circuit Makeup - Armadillo-460

6.3.6. CON9 (Expansion Interface 1) - Armadillo-460

CON9 is an expansion input/output interface. The signal layout is the same throughout the Armadillo-400 Series. Multiple functions are assigned to a single pin on this interface so that many different functions can be selected depending on the intended use. This is called multiplexing. For a description of the pin signals please refer to Table 6.25, “CON9 Signals - Armadillo-460”, for the multiplexed functions please refer to Table 6.26, “CON9 Signal Multiplex - Armadillo-460”, and for the initial state of each signal pin please refer to Appendix B, Initial Configuration State of Expansion Interfaces.

The signal layouts of CON8, CON9 and CON14 are the same throughout the Armadillo-400 Series, and the Armadillo-400 Series option modules can be used with either of Armadillo-420/440/460.

Table 6.25. CON9 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	EXT_IO0	In/Out	Expansion I/O 0, connected to VSTBY_REQ pin on i.MX257
2	EXT_IO1	In/Out	Expansion I/O 1, connected to RTCK pin on i.MX257
3	EXT_IO2	In/Out	Expansion I/O 2, connected to CSPI1_MOSI pin on i.MX257
4	EXT_IO3	In/Out	Expansion I/O 3, connected to CSI_D2 pin on i.MX257
5	EXT_IO4	In/Out	Expansion I/O 4, connected to CSPI1_MISO pin on i.MX257
6	EXT_IO5	In/Out	Expansion I/O 5, connected to CSI_D3 pin on i.MX257
7	+3.3V_IO	Power	Power (+3.3V_IO)
8	+3.3V_IO	Power	Power (+3.3V_IO)
9	GND	Power	Power (GND)
10	GND	Power	Power (GND)
11	EXT_IO6	In/Out	Expansion I/O 6, connected to CSPI1_SS1 pin on i.MX257
12	EXT_IO7	In/Out	Expansion I/O 7, connected to CSI_D4 pin on i.MX257
13	EXT_IO8	In/Out	Expansion I/O 8, connected to CSPI1_SCLK pin on i.MX257
14	EXT_IO9	In/Out	Expansion I/O 9, connected to CSI_D5 pin on i.MX257
15	EXT_IO10	In/Out	Expansion I/O 10, connected to CSI_D8 pin on i.MX257
16	EXT_IO11	In/Out	Expansion I/O 11, connected to CSI_D6 pin on i.MX257
17	EXT_IO12	In/Out	Expansion I/O 12, connected to CSI_D9 pin on i.MX257
18	EXT_IO13	In/Out	Expansion I/O 13, connected to CSI_D7 pin on i.MX257
19	GND	Power	Power (GND)
20	+3.3V_IO	Power	Power (+3.3V_IO)
21	EXT_IO14	In/Out	Expansion I/O 14, connected to CSI_MCLK pin on i.MX257
22	EXT_IO15	In/Out	Expansion I/O 15, connected to CSI_VSYNC pin on i.MX257
23	EXT_IO16	In/Out	Expansion I/O 16, connected to CSI_HSYNC pin on i.MX257
24	EXT_IO17	In/Out	Expansion I/O 17, connected to CSI_PIXCLK pin on i.MX257
25	EXT_IO18	In/Out	Expansion I/O 18, connected to CSPI1_SS0 pin on i.MX257
26	EXT_IO19	In/Out	Expansion I/O 19, connected to CSPI1_RDY pin on i.MX257
27	EXT_IO20	In/Out	Expansion I/O 20, connected to CLKO pin on i.MX257
28	EXT_IO21	In/Out	Expansion I/O 21, connected to EXT_ARMCLK pin on i.MX257

Table 6.26. CON9 Signal Multiplex - Armadillo-460

Pin Number	Function[a][b]										
	GPIO	CSPI1	CSPI3	UART3	UART5	SD2	CSI	AUD6	SIM1[c]	SIM2[c]	Other
1	GPIO3_17										
2	GPIO3_14										1-WIRE
3	GPIO1_14	MOSI		RXD							
4	GPIO1_27		MOSI		RXD	DAT4	D2		CLK0		
5	GPIO1_15	MISO		TXD							
6	GPIO1_28		MISO		TXD	DAT5	D3		RST0		
7											
8											
9											
10											
11	GPIO1_17	SS1		RTS							
12	GPIO1_29		SCLK		RTS	DAT6	D4		VEN0		
13	GPIO1_18	SCLK		CTS							
14	GPIO1_30		RDY		CTS	DAT7	D5		TX0		
15	GPIO1_7		SS2				D8	RXC		CLK0	
16	GPIO1_31		SS0			CMD	D6		PD0		
17	GPIO4_21		SS3				D9	RXFS		RST0	
18	GPIO1_6		SS1			CLK	D7		RX0		
19											
20											
21	GPIO1_8					DAT0	MCLK	TXD		VEN0	
22	GPIO1_9					DAT1	VSYNC	RXD		TX0	
23	GPIO1_10					DAT2	HSYNC	TXC		PD0	
24	GPIO1_11					DAT3	PIXCLK	TXFS		RX0	
25	GPIO1_16	SS0									PWMO2
26	GPIO2_22	RDY									
27	GPIO2_21										CLKO
28	GPIO3_15										

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

[c]As the SIM function has not be verified, there is no guarantee of its operation.

6.3.7. CON10 (i.MX257 JTAG Interface) - Armadillo-460

CON10 is an interface for connecting JTAG debuggers. It is connected to the JTAG Controller in the i.MX257.

It is possible to convert this interface to the standard ARM 20 pin layout with the Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00) option. For details, please see Appendix A, Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00).

Table 6.27. CON10 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	+3.3V_CPU	Power	Power (+3.3V_CPU)
2	JTAG_TRST*	In	Test Reset, connected to TRSTB pin on i.MX257
3	JTAG_TDI	In	Test Data In, connected to TDI pin on i.MX257
4	JTAG_TMS	In	Test Mode Select, connected to TMS pin on i.MX257
5	JTAG_TCK	In	Test Clock, connected to TCK pin on i.MX257
6	JTAG_TDO	Out	Test Data Out, connected to TDO pin on i.MX257
7	CPU_RESET*	In	i.MX257 reset[a], connected to RESET_B pin on i.MX257
8	GND	Power	Power (GND)

[a]Only i.MX257 is reset with the CPU_RESET* pin. If a full board reset is required, please use the EXT_RESET* pin on CON8.

The maximum output current of CON10 on Armadillo-460 is 200mA.

6.3.8. CON11 (LCD Expansion Interface) - Armadillo-460

CON11 is a LCD expansion interface which connects to LCD modules with digital RGB inputs. It has connections to a number of functions in the i.MX257, including the LCD controller and touch screen controller. For the signal pin layout please refer to Table 6.28, “CON11 Signals - Armadillo-460”, and for the initial state of each signal pin, please refer to Appendix B, Initial Configuration State of Expansion Interfaces.

- Max resolution: 800x600 (18bit)
- Supported touch screens: 4-Wire Resistive
- Connector Type: 50 pin FFC connector (0.5mm pitch)

The signal layout of CON11 is the same on Armadillo-440 and Armadillo-460, and the Armadillo-400 Series LCD Expansion Board can be used with both Armadillo-440 and Armadillo-460.

As CON11 is multiplexed many different functions can be selected. For information on the multiplexed functions, please refer to Table 6.29, “CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-460” and Table 6.30, “CON11 Signal Multiplexing (pins 39 - 50) - Armadillo-460”.

On Armadillo-460, it is possible to chose to connect the i.MX257 signals to either CON11 or CON19 with the equipped selector. For details, please refer to Figure 6.3, “CON11/CON19 Connection Selector - Armadillo-460”.

Connection selection with the selector is configured with the Ext I/F Control Register in the CPLD. For details on the CPLD memory map and registers, please refer to Appendix E, CPLD Registers - Armadillo-460.

Table 6.28. CON11 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	VIN	Power	Power (CON12 or CON13 power in[a])
2	VIN	Power	Power (CON12 or CON13 power in[a])
3	VIN	Power	Power (CON12 or CON13 power in[a])
4	+3.3V_IO	Power	Power (+3.3V_IO)
5	+3.3V_IO	Power	Power (+3.3V_IO)
6	GND	Power	Power (GND)
7	GND	Power	Power (GND)
8	LCD_LSCLK	Out	Connected to LSCLK pin on i.MX257
9	LCD_HSYN	Out	Connected to HSYNC pin on i.MX257
10	LCD_VSYN	Out	Connected to VSYNC pin on i.MX257
11	LCD_OE_ACD	Out	Connected to OE_ACD pin on i.MX257
12	PWMO1	Out	Connected to PWM pin on i.MX257
13	LCD_LD0	Out	Connected to LD0 pin on i.MX257
14	LCD_LD1	Out	Connected to LD1 pin on i.MX257
15	LCD_LD2	Out	Connected to LD2 pin on i.MX257
16	LCD_LD3	Out	Connected to LD3 pin on i.MX257
17	LCD_LD4	Out	Connected to LD4 pin on i.MX257
18	LCD_LD5	Out	Connected to LD5 pin on i.MX257
19	GND	Power	Power (GND)
20	LCD_LD6	Out	Connected to LD6 pin on i.MX257
21	LCD_LD7	Out	Connected to LD7 pin on i.MX257
22	LCD_LD8	Out	Connected to LD8 pin on i.MX257
23	LCD_LD9	Out	Connected to LD9 pin on i.MX257
24	LCD_LD10	Out	Connected to LD10 pin on i.MX257
25	LCD_LD11	Out	Connected to LD11 pin on i.MX257
26	GND	Power	Power (GND)
27	LCD_LD12	Out	Connected to LD12 pin on i.MX257
28	LCD_LD13	Out	Connected to LD13 pin on i.MX257
29	LCD_LD14	Out	Connected to LD14 pin on i.MX257
30	LCD_LD15	Out	Connected to LD15 pin on i.MX257
31	LCD_LD16	Out	Connected to GPIO_E pin on i.MX257
32	LCD_LD17	Out	Connected to GPIO_F pin on i.MX257
33	GND	Power	Power (GND)
34	TOUCH_XP	In/Out	Connected to XP pin on i.MX257
35	TOUCH_XN	In/Out	Connected to XN pin on i.MX257
36	TOUCH_YP	In/Out	Connected to YP pin on i.MX257
37	TOUCH_YN	In/Out	Connected to YN pin on i.MX257
38	GND	Power	Power (GND)
39	EXT_IO24	In/Out	Expansion I/O 24, connected to DE_B pin on i.MX257
40	EXT_IO25	In/Out	Expansion I/O 25, connected to KPP_ROW0 pin on i.MX257
41	EXT_IO26	In/Out	Expansion I/O 26, connected to KPP_ROW1 pin on i.MX257
42	EXT_IO27	In/Out	Expansion I/O 27, connected to KPP_ROW2 pin on i.MX257
43	EXT_IO28	In/Out	Expansion I/O 28, connected to KPP_ROW3 pin on i.MX257
44	EXT_IO29	In/Out	Expansion I/O 29, connected to KPP_COL0 pin on i.MX257
45	EXT_IO30	In/Out	Expansion I/O 30, connected to KPP_COL1 pin on i.MX257
46	EXT_IO31	In/Out	Expansion I/O 31, connected to KPP_COL2 pin on i.MX257
47	EXT_IO32	In/Out	Expansion I/O 32, connected to KPP_COL3 pin on i.MX257
48	EXT_IO33	In/Out	Expansion I/O 33, connected to GPIO_A pin on i.MX257
49	EXT_IO34	In/Out	Expansion I/O 34, connected to GPIO_B pin on i.MX257

Pin Number	Signal Name	I/O	Function
50	GND	Power	Power (GND)

[a]Connected via a polyswitch fuse to J1/J2 power (+5V).

Table 6.29. CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-460

Pin Number	Function[a][b]					
	LCDC	SLCDC	ADC	SIM1[c]	SIM2[c]	Other
1						
2						
3						
4						
5						
6						
7						
8	LSCLK	CS			PD1	
9	HSYN				VEN1	
10	VSYN				TX1	
11	OE_ACD	RS			RX1	
12						PWMO1
13	LD0	D0		CLK1		
14	LD1	D1		RST1		
15	LD2	D2		VEN1		
16	LD3	D3		TX1		
17	LD4	D4		PD1		
18	LD5	D5		RX1		
19						
20	LD6	D6			CLK1	
21	LD7	D7			RST1	
22	LD8	D8				
23	LD9	D9				
24	LD10	D10				
25	LD11	D11				
26						
27	LD12	D12				
28	LD13	D13				
29	LD14	D14				
30	LD15	D15				
31	LD16					
32	LD17					
33						
34			XP			
35			XN			
36			YP			
37			YN			
38						

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

[c]As the SIM function has not be verified, there is no guarantee of its operation.

Table 6.30. CON11 Signal Multiplexing (pins 39 - 50) - Armadillo-460

Pin Number	Function[a][b][c]							
	GPIO	UART3	UART4	AUD5	KPP	I2C3	CAN1	Other
39	GPIO2_20							

Pin Number	Function[a][b][c]							
	GPIO	UART3	UART4	AUD5	KPP	I2C3	CAN1	Other
40	GPIO2_29	RTD			ROW0			
41	GPIO2_30	TXD			ROW1			
42	GPIO2_31	RTS		RXC	ROW2			
43	GPIO3_0	CTS		RXFS	ROW3			
44	GPIO3_1		RXD	TXD	COL0			
45	GPIO3_2		TXD	RXD	COL1			
46	GPIO3_3		RTS	TXC	COL2			
47	GPIO3_4		CTS	TXFS	COL3			
48	GPIO1_0				ROW4	SCL	TX	PWMO2
49	GPIO1_1				ROW5	SDA	RX	PWMO3
50								

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

[c]On Armadillo-460, the signals of CON11 pins 44 - 47 and CON19 (serial I/F) can be selected exclusively of each other with the CPLD registers.

6.3.9. CON12, CON13 (Power In) - Armadillo-460

CON12 is a power in connector for the included AC adapter conversion cable on Armadillo-460. The AC adapter jack type is EIAJ RC-5320A compliant (voltage classification 2). Jacks with the same polarity mark as Figure 6.6, “AC Adapter Polarity Mark - Armadillo-460” can be used.

Figure 6.6. AC Adapter Polarity Mark - Armadillo-460

Table 6.31. CON12 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	VIN	Power	Power in connector
2	GND	Power	Power (GND)
3	GND	Power	Power (GND)
4	+12V	Power	Power in connector

On Armadillo-460 CON12 accepts a power in voltage range of DC4.75V to 5.25V. Do not apply a voltage higher than 5.25V as this may damage the internal devices.

On Armadillo-460, as the power lines (+5V) of CON12 and J1/J2 are connected by a polyswitch fuse they cannot both be used at the same time. Please be sure to only supply power with one of the connectors.

+12V of CON12 is supplied to the Expansion Bus Interface and is not used for internal circuits on Armadillo-460. If the +12V is not being used by a PC/104 board connected to the Expansion Bus Interface, it does not need to be connected. Please refer to Figure 3.5, “Armadillo-460 Power Circuit Make-up Diagram” for details.

CON13 is a connector for suppling power to PC/104 boards which connect to the Expansion Bus Interface. Signal lines for control of the power management IC (PMIC) on/off and the external backup power in of the real-time clock on Armadillo-460 are included in this connector.

Table 6.32. CON13 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	GND	Power	Power (GND)
2	BAT	Power	Real-time clock external backup power in
3	GND	Power	Power (GND)
4	PMIC_ONOFF*	In	PMIC ON/OFF control (2sec or longer GND short to power off, GND short again to power back on)[a][b]
5	GND	Power	Power (GND)
6	-5V	Power	Power in connector
7	GND	Power	Power (GND)
8	-12V	Power	Power in connector

[a]PMIC_ONOFF* has a 10kΩ pull-up from power in VIN

[b]This is in a wired OR connection to RTC alarm 2 interrupt output on Armadillo-460.

On Armadillo-460, as CON13 and J1 are connected by a polyswitch fuse they cannot both be used at the same time. Please be sure to only supply power with one of the connectors.

CON13 (pin 2) accepts a power in voltage range of DC1.5V to 3.5V. Do not apply a voltage higher than 3.5V as the internal devices may stop functioning properly.

After the board has been powered off with the PMIC_ONOFF* signal, when disconnecting and then soon reconnecting the power supply to CON12 the PMIC will not power back on and the board will not boot. The board can be booted by shorting the PMIC_ONOFF* signal to GND.

-5V/-12V of CON13 is supplied to the Expansion Bus Interface and is not used for internal circuits on Armadillo-460. If the -5V/-12V is not being used by a PC/104 board connected to the Expansion Bus Interface, it does not need to be connected. Please refer to Figure 3.5, “Armadillo-460 Power Circuit Make-up Diagram” for details.

6.3.10. CON14 (Expansion Interface 2) - Armadillo-460

CON14 is an expansion input/output interface. Multiple functions are assigned to a single pin so that many different functions can be selected depending on the intended use. For a description of the pin signals please refer to Table 6.34, “CON14 Signal Multiplex - Armadillo-460”, for the multiplexed functions please refer to Table 6.34, “CON14 Signal Multiplex - Armadillo-460”, and for the initial state of each signal pin please refer to Appendix B, Initial Configuration State of Expansion Interfaces.

The signal layouts of CON8, CON9 and CON14 are the same throughout the Armadillo-400 Series, and the Armadillo-400 Series option modules can be used with either of Armadillo-420/440/460.

Table 6.33. CON14 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	+3.3V_IO	Power	Power (+3.3V_IO)
2	GND	Power	Power (GND)
3	EXT_IO22	In/Out	Expansion I/O 22, connected to GPIO_C pin on i.MX257
4	EXT_IO23	In/Out	Expansion I/O 23, connected to GPIO_D pin on i.MX257

Table 6.34. CON14 Signal Multiplex - Armadillo-460

Pin Number	Function[a][b]				
	GPIO	CSPI1	I2C2	CAN2	Other
1					
2					
3	GPIO1_2	SS2	SCL	TX	PWMO4
4	GPIO1_3		SDA	RX	

[a]For details on the multiplexing, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

[b]Different multiplexing can be set for each individual pin.

6.3.11. CON20 (External RTC Backup Power In) - Armadillo-460

CON20 on Armadillo-460 is a real-time clock (RTC) external backup power in connector. It is possible to connect a separate external battery such as WK11 (Hitachi Maxell) or similar in order to maintain time data during extended periods of no power supply.

Table 6.35. CON20 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	VDD	Power	Power in connector
2	GND	Power	Power (GND)

CON20 accepts a power in voltage range of 1.5V to 3.5V. Do not apply a voltage higher than 3.5V as the internal devices may stop functioning properly.

6.3.12. CON21 (Power Out) - Armadillo-460

CON21 on Armadillo-460 is a connector to supply power to external devices.

Table 6.36. CON21 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	VDD	Power	Power (+3.3V_EXT[a])
2	VDD	Power	Power (+3.3V_EXT[a])
3	GND	Power	Power (GND)

Pin Number	Signal Name	I/O	Function
4	-	-	-

[a]The combined maximum output current of CON1, CON4, CON7, CON19, CON21, CON23 and CON25 on Armadillo-460 is 500mA.

6.3.13. J1, J2 (Expansion Bus Interface) - Armadillo-460

J1、J2 is the Expansion Bus Interface. Three different modes can be selected by configuring the internal registers of the i.MX257 and CPLD. Please refer to Section 6.3.13.3, “Expansion Bus Makeup - Armadillo-460” for details.

For details on the registers in the i.MX257, please refer to the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

- PC/104 Expansion Bus Compatibility Mode
- Direct CPU Bus Mode (Asynchronous)
- Direct CPU Bus Mode (Synchronous)

Armadillo-460 was developed based on the PC/104 Specification Version 2.6. Please refer to http://www.pc104.org for information on the PC/104 standard.

6.3.13.1. PC/104 Expansion Bus Compatibility Mode Signals - Armadillo-460

The signals for when the PC/104 expansion bus compatibility mode is selected are as follows.

Table 6.37. PC/104 Expansion Bus Compatibility Mode J1 Signals (1) - Armadillo-460

Pin Number	Signal Name	I/O	Function
A1	IOCHK*	(In)	Not supported (not connected)[a]
A2	SD7	In/Out	Data bus (bit 7)
A3	SD6	In/Out	Data bus (bit 6)
A4	SD5	In/Out	Data bus (bit 5)
A5	SD4	In/Out	Data bus (bit 4)
A6	SD3	In/Out	Data bus (bit 3)
A7	SD2	In/Out	Data bus (bit 2)
A8	SD1	In/Out	Data bus (bit 1)
A9	SD0	In/Out	Data bus (bit 0)
A10	IOCHRDY	In	Access cycle lengthening (1kΩ pull-up by V_PC104)[a]
A11	AEN	Out	Bus release (GND)
A12	SA19	Out	Address bus (bit 19)
A13	SA18	Out	Address bus (bit 18)
A14	SA17	Out	Address bus (bit 17)
A15	SA16	Out	Address bus (bit 16)
A16	SA15	Out	Address bus (bit 15)
A17	SA14	Out	Address bus (bit 14)
A18	SA13	Out	Address bus (bit 13)
A19	SA12	Out	Address bus (bit 12)
A20	SA11	Out	Address bus (bit 11)
A21	SA10	Out	Address bus (bit 10)
A22	SA9	Out	Address bus (bit 9)
A23	SA8	Out	Address bus (bit 8)
A24	SA7	Out	Address bus (bit 7)
A25	SA6	Out	Address bus (bit 6)
A26	SA5	Out	Address bus (bit 5)
A27	SA4	Out	Address bus (bit 4)
A28	SA3	Out	Address bus (bit 3)

Pin Number	Signal Name	I/O	Function
A29	SA2	Out	Address bus (bit 2)
A30	SA1	Out	Address bus (bit 1)
A31	SA0	Out	Address bus (bit 0)
A32	GND	Power	Power (GND)

[a]Information on pull-ups and pull-downs for logic fixing and unconnected signal lines is shown in brackets. All logic fixing is done with resistors on the Armadillo-460 board.

Table 6.38. PC/104 Expansion Bus Compatibility Mode J1 Signals (2) - Armadillo-460

Pin Number	Signal Name	I/O	Function
B1	GND	Power	Power (GND)
B2	RESET	Out	Reset Output
B3	+5V	Power	Power (+5V)
B4	IRQ9	In	Interrupt request 9 (10kΩ pull-up by V_PC104)[a]
B5	-5V	Power	Power (-5V)
B6	DRQ2	(In)	Not supported (not connected)[a]
B7	-12V	Power	Power (-12V)
B8	SRDY*	(In)	Not supported (300Ω pull-up by V_PC104)[a]
B9	+12V	Power	Power (+12V)
B10	KEY	-	GND
B11	SMEMW*	Out	Memory write strobe
B12	SMEMR*	Out	Memory read strobe
B13	IOW*	Out	Write strobe
B14	IOR*	Out	Read strobe
B15	DACK3*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
B16	DRQ3	(In)	Not supported (not connected)[a]
B17	DACK1*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
B18	DRQ1	(In)	Not supported (not connected)[a]
B19	REFRESH*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
B20	BCLK	Out	8.3MHz (1/16 of BUS clock 133MHz)
B21	IRQ7	In	Interrupt request 7 (10kΩ pull-up by V_PC104)[a]
B22	IRQ6	In	Interrupt request 6 (10kΩ pull-up by V_PC104)[a]
B23	IRQ5	In	Interrupt request 5 (10kΩ pull-up by V_PC104)[a]
B24	IRQ4	In	Interrupt request 4 (10kΩ pull-up by V_PC104)[a]
B25	IRQ3	In	Interrupt request 3 (10kΩ pull-up by V_PC104)[a]
B26	DACK2*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
B27	TC	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
B28	BALE	Out	Address latch enable
B29	+5V	Power	Power (+5V)
B30	OSC	(Out)	Not supported (not connected)[a]
B31	GND	Power	Power (GND)
B32	GND	Power	Power (GND)

[a]Information on pull-ups and pull-downs for logic fixing and unconnected signal lines is shown in brackets. All logic fixing is done with resistors on the Armadillo-460 board.

Table 6.39. PC/104 Expansion Bus Compatibility Mode J2 Signals (1) - Armadillo-460

Pin Number	Signal Name	I/O	Function
C0	GND	Power	Power (GND)
C1	SBHE*	Out	Bus high enable (active when using upper 8bits of data bus)
C2	LA23	Out	Address bus (bit 23)
C3	LA22	Out	Address bus (bit 22)
C4	LA21	Out	Address bus (bit 21)
C5	LA20	Out	Address bus (bit 20)

Pin Number	Signal Name	I/O	Function
C6	LA19	Out	Address bus (bit 19)
C7	LA18	Out	Address bus (bit 18)
C8	LA17	Out	Address bus (bit 17)
C9	MEMR*	Out	Memory read strobe
C10	MEMW*	Out	Memory write strobe
C11	SD8	In/Out	Data bus (bit 8)
C12	SD9	In/Out	Data bus (bit 9)
C13	SD10	In/Out	Data bus (bit 10)
C14	SD11	In/Out	Data bus (bit 11)
C15	SD12	In/Out	Data bus (bit 12)
C16	SD13	In/Out	Data bus (bit 13)
C17	SD14	In/Out	Data bus (bit 14)
C18	SD15	In/Out	Data bus (bit 15)
C19	KEY	-	GND

Table 6.40. PC/104 Expansion Bus Compatibility Mode J2 Signals (2) - Armadillo-460

Pin Number	Signal Name	I/O	Function
D0	GND	Power	Power (GND)
D1	MEMCS16*	(In)	Not supported (300Ω pull-up by V_PC104)[a]
D2	IOCS16*	(In)	Not supported (300Ω pull-up by V_PC104)[a]
D3	IRQ10	In	Interrupt request 10 (10kΩ pull-up by V_PC104)[a]
D4	IRQ11	In	Interrupt request 11 (10kΩ pull-up by V_PC104)[a]
D5	IRQ12	In	Interrupt request 12 (10kΩ pull-up by V_PC104)[a]
D6	IRQ15	In	Interrupt request 15 (10kΩ pull-up by V_PC104)[a]
D7	IRQ14	In	Interrupt request 14 (10kΩ pull-up by V_PC104)[a]
D8	DACK0*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
D9	DRQ0	(In)	Not supported (not connected)[a]
D10	DACK5*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
D11	DRQ5	(In)	Not supported (not connected)[a]
D12	DACK6*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
D13	DRQ6	(In)	Not supported (not connected)[a]
D14	DACK7*	(Out)	Not supported (10kΩ pull-up by V_PC104)[a]
D15	DRQ7	(In)	Not supported (not connected)[a]
D16	+5V	Power	Power (+5V)
D17	MASTER16*	(In)	Not supported (300Ω pull-up by V_PC104)[a]
D18	GND	Power	Power (GND)
D19	GND	Power	Power (GND)

[a]Information on pull-ups and pull-downs for logic fixing and unconnected signal lines is shown in brackets. All logic fixing is done with resistors on the Armadillo-460 board.

6.3.13.2. Direct CPU Bus Mode Signals - Armadillo-460

The signals for when the direct CPU bus mode is selected are as follows.

Table 6.41. Direct CPU Bus Compatibility Mode J1 Signals (1) - Armadillo-460

Pin Number	Signal Name	I/O	Function
A1	-	-	Reserved (not connected)[a]
A2	SD7	In/Out	Data bus (bit 7)
A3	SD6	In/Out	Data bus (bit 6)
A4	SD5	In/Out	Data bus (bit 5)
A5	SD4	In/Out	Data bus (bit 4)
A6	SD3	In/Out	Data bus (bit 3)
A7	SD2	In/Out	Data bus (bit 2)

Pin Number	Signal Name	I/O	Function
A8	SD1	In/Out	Data bus (bit 1)
A9	SD0	In/Out	Data bus (bit 0)
A10	DTACK*	In	Asynchronous: Wait signal, connected to DTACK* pin on i.MX257 (1kΩ pull-up by V_PC104) [a]
	RDY*		Synchronous: Ready signal, connected to DTACK* pin on i.MX257 (1kΩ pull-up by V_PC104)[a]
A11	-	-	Reserved (GND)
A12	SA19	Out	Address bus (bit 19)
A13	SA18	Out	Address bus (bit 18)
A14	SA17	Out	Address bus (bit 17)
A15	SA16	Out	Address bus (bit 16)
A16	SA15	Out	Address bus (bit 15)
A17	SA14	Out	Address bus (bit 14)
A18	SA13	Out	Address bus (bit 13)
A19	SA12	Out	Address bus (bit 12)
A20	SA11	Out	Address bus (bit 11)
A21	SA10	Out	Address bus (bit 10)
A22	SA9	Out	Address bus (bit 9)
A23	SA8	Out	Address bus (bit 8)
A24	SA7	Out	Address bus (bit 7)
A25	SA6	Out	Address bus (bit 6)
A26	SA5	Out	Address bus (bit 5)
A27	SA4	Out	Address bus (bit 4)
A28	SA3	Out	Address bus (bit 3)
A29	SA2	Out	Address bus (bit 2)
A30	SA1	Out	Address bus (bit 1)
A31	SA0	Out	Address bus (bit 0)
A32	GND	Power	Power (GND)

[a]Information on pull-ups and pull-downs for logic fixing and unconnected signal lines is shown in brackets. All logic fixing is done with resistors on the Armadillo-460 board.

Table 6.42. Direct CPU Bus Compatibility Mode J1 Signals (2) - Armadillo-460

Pin Number	Signal Name	I/O	Function
B1	GND	Power	Power (GND)
B2	RESET	Out	Reset Output
B3	+5V	Power	Power (+5V)
B4	IRQ9	In	Interrupt request 9 (10kΩ pull-up by V_PC104)[a]
B5	-5V	Power	Power (-5V)
B6	-	-	Reserved (not connected)[a]
B7	-12V	Power	Power (-12V)
B8	-	-	Reserved (300Ω pull-up by V_PC104)[a]
B9	+12V	Power	Power (+12V)
B10	-	-	Reserved (GND)
B11	RW*	Out	Read-write, connected to RW* on i.MX257
B12	OE*	Out	Output enable, connected to OE* on i.MX257
B13	CS4*	Out	Chip Select 4, connected to CS4* on i.MX257
B14	CS3*	Out	Chip Select 3, connected to CS3* on i.MX257
B15	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
B16	-	-	Reserved (not connected)[a]
B17	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
B18	-	-	Reserved (not connected)[a]
B19	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
B20	SYSCLK	Out	66MHz (1/2 of BUS Clock 133MHz)
B21	IRQ7	In	Interrupt request 7 (10kΩ pull-up by V_PC104)[a]

Pin Number	Signal Name	I/O	Function
B22	IRQ6	In	Interrupt request 6 (10kΩ pull-up by V_PC104)[a]
B23	IRQ5	In	Interrupt request 5 (10kΩ pull-up by V_PC104)[a]
B24	IRQ4	In	Interrupt request 4 (10kΩ pull-up by V_PC104)[a]
B25	IRQ3	In	Interrupt request 3 (10kΩ pull-up by V_PC104)[a]
B26	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
B27	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
B28	-	-	Reserved (GND)
B29	+5V	Power	Power (+5V)
B30	-	-	Reserved (not connected)
B31	GND	Power	Power (GND)
B32	GND	Power	Power (GND)

[a]Information on pull-ups and pull-downs for logic fixing and unconnected signal lines is shown in brackets. All logic fixing is done with resistors on the Armadillo-460 board.

Table 6.43. Direct CPU Bus Compatibility Mode J2 Signals (1) - Armadillo-460

Pin Number	Signal Name	I/O	Function
C0	GND	Power	Power (GND)
C1	EB1*	Out	Enable Byte 1 Connected to EB1* on i.MX257 (active when using upper 8bits of data bus)
C2	SA23	Out	Address bus (bit 23)
C3	SA22	Out	Address bus (bit 22)
C4	SA21	Out	Address bus (bit 21)
C5	SA20	Out	Address bus (bit 20)
C6	SA19	Out	Address bus (bit 19)
C7	SA18	Out	Address bus (bit 18)
C8	SA17	Out	Address bus (bit 17)
C9	OE*	Out	Output enable, connected to OE* on i.MX257
C10	RW*	Out	Read-write, connected to RW* on i.MX257
C11	SD8	In/Out	Data bus (bit 8)
C12	SD9	In/Out	Data bus (bit 9)
C13	SD10	In/Out	Data bus (bit 10)
C14	SD11	In/Out	Data bus (bit 11)
C15	SD12	In/Out	Data bus (bit 12)
C16	SD13	In/Out	Data bus (bit 13)
C17	SD14	In/Out	Data bus (bit 14)
C18	SD15	In/Out	Data bus (bit 15)
C19	-	-	Reserved (GND)

Table 6.44. Direct CPU Bus Compatibility Mode J2 Signals (2) - Armadillo-460

Pin Number	Signal Name	I/O	Function
D0	GND	Power	Power (GND)
D1	-	-	Reserved (300Ω pull-up by V_PC104)[a]
D2	-	-	Reserved (300Ω pull-up by V_PC104)[a]
D3	IRQ10	In	Interrupt request 10 (10kΩ pull-up by V_PC104)[a]
D4	IRQ11	In	Interrupt request 11 (10kΩ pull-up by V_PC104)[a]
D5	IRQ12	In	Interrupt request 12 (10kΩ pull-up by V_PC104)[a]
D6	IRQ15	In	Interrupt request 15 (10kΩ pull-up by V_PC104)[a]
D7	IRQ14	In	Interrupt request 14 (10kΩ pull-up by V_PC104)[a]
D8	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
D9	-	-	Reserved (not connected)[a]
D10	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
D11	Reserved	-	Not connected

Pin Number	Signal Name	I/O	Function
D12	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
D13	-	-	Reserved (not connected)[a]
D14	-	-	Reserved (10kΩ pull-up by V_PC104)[a]
D15	-	-	Reserved (not connected)[a]
D16	+5V	Power	Power (+5V)
D17	-	-	Reserved (300Ω pull-up by V_PC104)[a]
D18	GND	Power	Power (GND)
D19	GND	Power	Power (GND)

[a]Information on pull-ups and pull-downs for logic fixing and unconnected signal lines is shown in brackets. All logic fixing is done with resistors on the Armadillo-460 board.

6.3.13.3. Expansion Bus Makeup - Armadillo-460

The expansion bus on Armadillo-460 is implemented using a CPLD. For information on the CPLD memory map and registers, please refer to Appendix E, CPLD Registers - Armadillo-460.

6.3.13.3.1. Interrupts

The Armadillo-460 expansion bus interrupt controller is built into the CPLD and is connected to the IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14 and IRQ15 interrupt signals.

The detectable interrupt types are show in Table 6.45, “Interrupt Detection Types”. The interrupt type (LEVEL-HIGH, LEVEL-LOW, RISING-EDGE or FALLING-EDGE) can be selected for interrupts IRQ3 to IRQ7 and IRQ9 to IRQ11. Interrupts IRQ12, IRQ14 and IRQ15 are fixed LEVEL-HIGH.

Table 6.45. Interrupt Detection Types

IRQ Number	LEVEL-HIGH	LEVEL-LOW	FALLING-EDGE	RISING-EDGE
IRQ3	Yes	Yes	Yes	Yes
IRQ4	Yes	Yes	Yes	Yes
IRQ5	Yes	Yes	Yes	Yes
IRQ6	Yes	Yes	Yes	Yes
IRQ7	Yes	Yes	Yes	Yes
IRQ9	Yes	Yes	Yes	Yes
IRQ10	Yes	Yes	Yes	Yes
IRQ11	Yes	Yes	Yes	Yes
IRQ12	Yes	No	No	No
IRQ14	Yes	No	No	No
IRQ15	Yes	No	No	No

The mechanism of the interrupt controller is shown in Figure 6.7, “Interrupt Controller Mechanism”. The interrupt detection types of IRQ3 to IRQ7 and IRQ9 to IRQ11 can be selected with the Ext Interrupt Polarity Type Register (POL) and the Ext Interrupt Detection Type Register (DET). When the interrupt detection type is set to LEVEL, the value is used as is, and when it is set to EDGE, the value stored by the flip-flop (FF) is used. The FF value is saved until the CLR signal is activated. The interrupt status can be obtained from the Ext Interrupt Status Register (IRQ). The interrupt signals are masked by the Interrupt Mask Register (MASK) and then the OR of all interrupt signals is used to signal interrupts to the CPU.

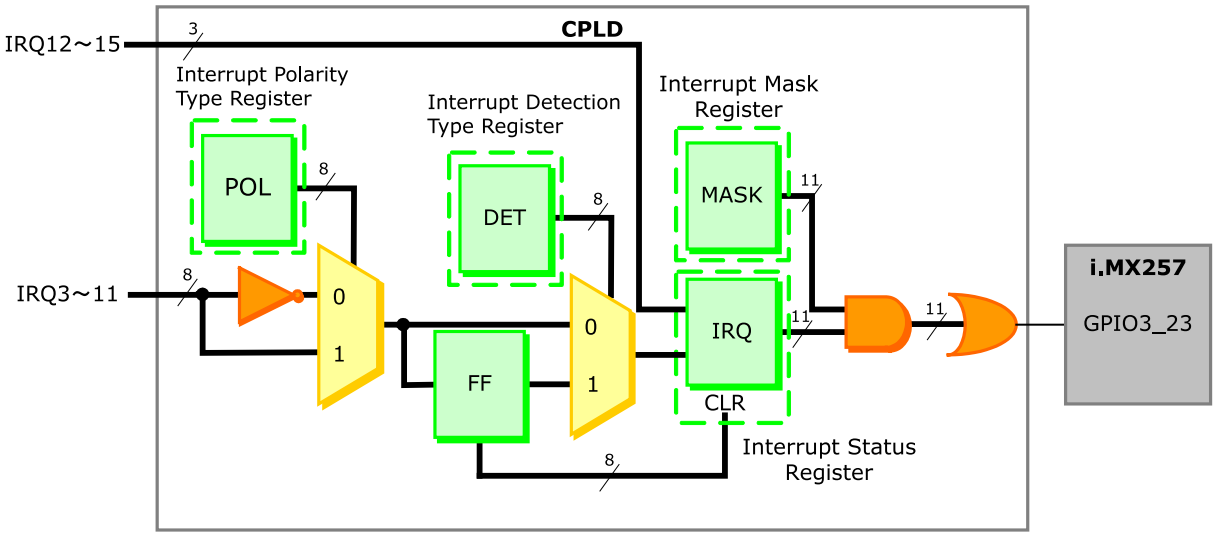


Figure 6.7. Interrupt Controller Mechanism

6.3.13.3.2. Expansion Bus Mode Configuration

The following three modes can be selected with the Ext Control Register for the expansion bus on Armadillo-460.

- PC/104 Expansion Bus Compatibility Mode
- Direct CPU Bus Mode (Asynchronous)
- Direct CPU Bus Mode (Synchronous)

6.3.13.3.2.1. PC/104 Expansion Bus Compatibility Mode

When set to PC/104 expansion bus compatibility mode, J1 and J2 take on a PC/104 bus signal layout and have a 64KB I/O space and a 16MB memory space. However, as the ARM architecture does not have a I/O space (for I/O only access) like that of x86 CPUs, the I/O space is assigned to regular memory space. Also, as it only supports a subset of the PC/104 standard, the following functions normally held by a PC/104 bus are not supported.

- Dynamic Bus Sizing Function
- DMA (DREQ/DACK) Function
- External Master Function

As the PC/104 expansion bus compatibility mode does not have dynamic bus sizing functionality, special caution must be taken when accessing the PC/104 I/O and memory space. Both the 64KB I/O physical address space and the 16MB memory physical address space can be accessed by two (8bit and 16bit) virtual address spaces. The same physical address space is accessed when either one of the virtual address spaces is accessed.

Due to the Errata ENGcm11270 limitation, A[23] cannot be used when AUS (Address Unshifted mode) is specified. Because of this, the address space is limited to 8MByte in some instances depending on the PC/104 expansion bus mode and the direct CPU bus mode configuration. For the usable address space in each mode, please refer to Table 4.1, “Physical Memory Map - Armadillo-420/440” and Table 4.3, “CS3/CS4 Space Accessible in Direct CPU Bus Mode”. For information

on this errata, please refer to "ENGcm11270" in "Chip Errata for the i.MX25" from the /document/datasheet/ directory on the included DVD.

The use of each virtual address space is as shown below.

8bit Virtual Address Space	• 8bit access with data bus (SD7 to SD0)
16bit Virtual Address Space	• 8bit access to odd addresses with data bus (SD15 to SD8) • 8bit access to even addresses with data bus (SD7 to SD0) • 16bit access with data bus (SD15 - SD0)

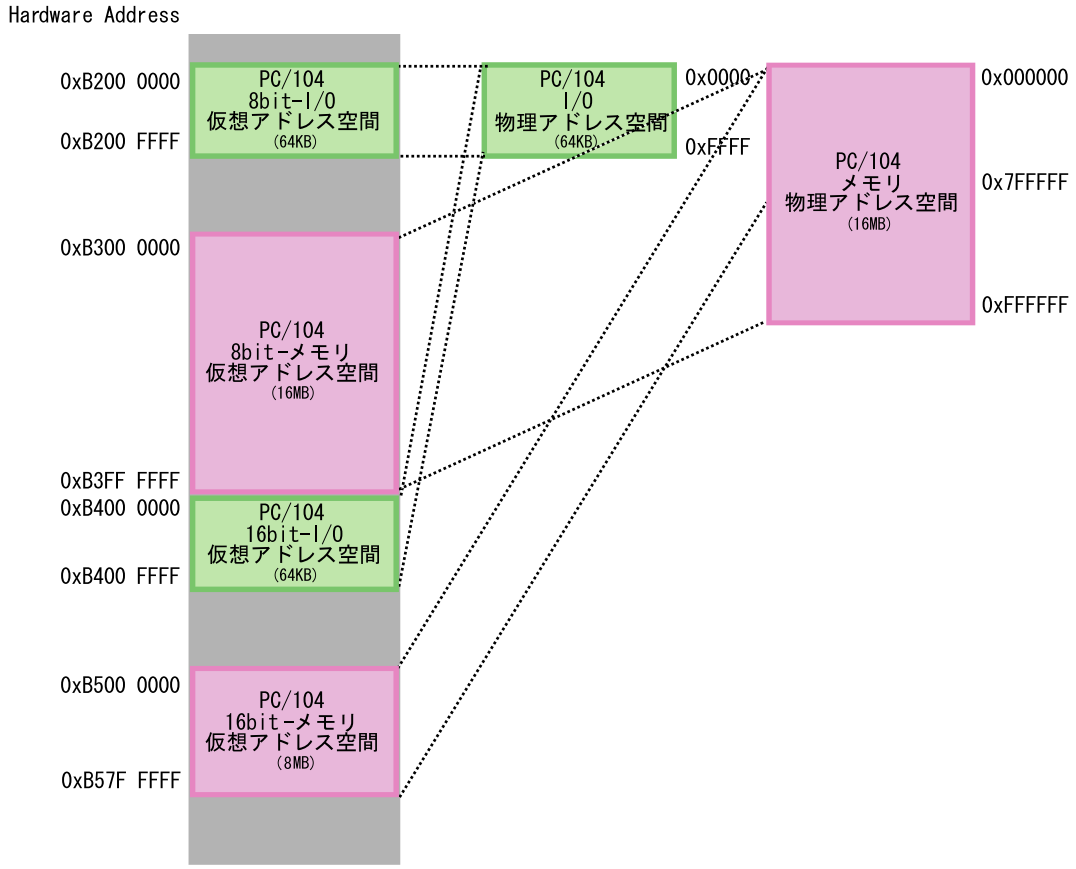


Figure 6.8. PC/104 Expansion Bus Compatibility Mode Memory Space

Due to the Errata ENGcm11270 limitation, A[23] cannot be used when AUS (Address Unshifted mode) is specified.

Because of this, access to 8MByte of the physical address space is limited when the physical address space is accessed from the 16bit memory virtual address space. To access the 16MB physical address space, please access it from the 8bit memory virtual address space.

For information on this errata, please refer to "ENGcm11270" in "Chip Errata for the i.MX25" from the /document/datasheet/ directory on the included DVD.

The address to access the physical address space can be calculated with Base Address + Offset Address as shown below.

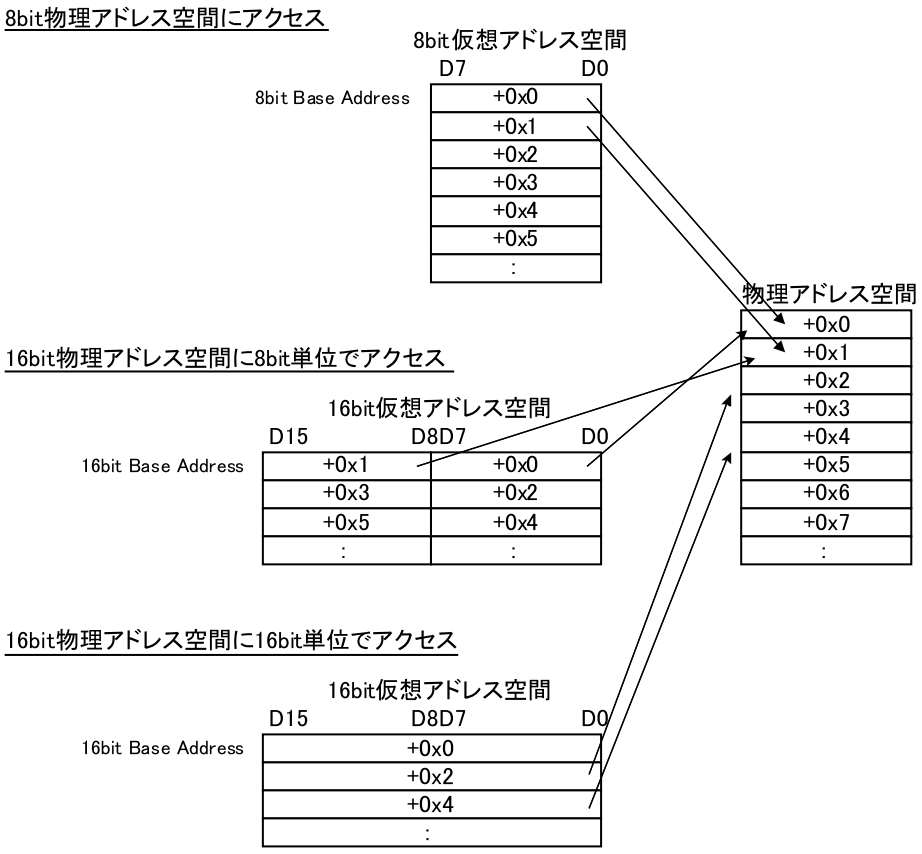


Figure 6.9. PC/104 Expansion Bus Compatibility Mode Bus Access

SBHE* is an Active-Low signal that shows that the data bus (SD15 to SD8) is being used. The relationship between data access and SBHE* is shown in Table 6.46, “SBHE* and Data Access Relationship”.

Please note that while data bus (SD7 to SD0) is used for lower 8bit read accesses, SBHE* will have a low level.

Table 6.46. SBHE* and Data Access Relationship

Data	Access	SBHE*
16bit (SD15 - SD0)	Read	Low
	Write	
Higher 8bit (SD15 - SD8)	Read	Low
	Write	
Lower 8bit (SD7 - SD0)	Read	Low
	Write	High

The bus access timing of the PC/104 Expansion Bus Compatibility Mode is as follows.

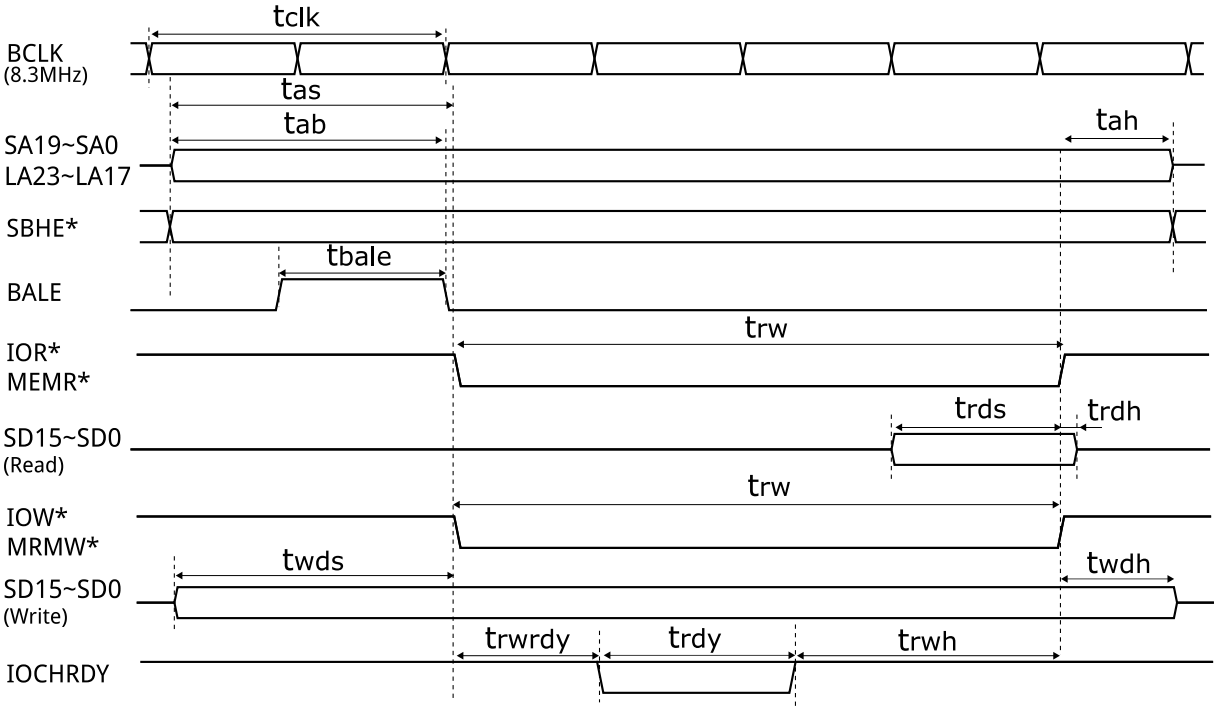


Figure 6.10. PC/104 Expansion Bus Compatibility Mode Bus Access Timing

BCLK is a 8.3MHz clock output. The access cycle can be lengthened by asserting IOCHRDY within 70ns of asserting IOR*, IOW*, MEMR* and MEMW*. The pulse width of IOR*, MEMR*, IOW* and MEMW* can be changed with WSC. It is normally set to approximately 240ns (WSC=25), but can be changed between approximately 120ns (WSC=9) to 518ns (WSC=62).

For details on the WSC, please refer to "Chapter 49 Wireless External Interface Module" in the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

Table 6.47. PC/104 Expansion Bus Compatibility Mode Bus Access Timing

Symbol	Explanation	min (ns)	max (ns)	Notes
t_{clk}	BCLK period	120		
t_{as}	SA, LA and SBHE* setup time for IOR*, MEMR*, IOW* and MEMW* asserts	124		
t_{ab}	SA, LA and SBHE* setup time for BALE de-assert	124		
t_{ah}	SA, LA and SBHE* hold time for IOR*, MEMR*, IOW* and MEMW* asserts	33		
t_{bale}	BALE pulse width	75		
t_{rw}	IOR*, MEMR*, IOW* and MEMW* pulse width	120	525	240ns (typ.) on factory image (WSC+1) x 7.5-45ns (typ.)
t_{rds}	SD setup time for reads	32		
t_{rdh}	SD hold time for reads	0		
t_{wds}	SD setup time for writes	103		
t_{wdh}	SD hold time for writes	32		
t_{rwrdy}	IOCHRDY assert effective time for IOR*, MEMR*, IOW* and MEMW*		70	
t_{rdy}	IOCHRDY pulse width	125	(7470-WSCx7.5)/ n[a]	System reset will occur if max value is exceeded
t_{rwh}	IOR*, MEMR*, IOW* and MEMW* hold time for IOCHRDY de-assert	22	428	(WSC+1) x 7.5-56.3ns (typ.)

[a]n = continuous access cycles (ex. word access to 8bit space: n = 4, half-word access: n = 2)

6.3.13.3.2.2. Direct CPU Bus Mode (Asynchronous)

Direct CPU Bus Mode (Asynchronous) takes on the CS3 (0xB2000000 - 0xB3FFFFFF) and CS4 (0xB4000000 - 0xB5FFFFFF) memory spaces. Data widths of 8bit and 16bit can be selected by configuring the Wireless External Interface Module(WEIM). 66MHz is output from SYSCLK, and EB1*, CS3*, CS4*, OE* and RW* are output as is. The access cycle can be lengthened with DTACK*.

For details on the configuration of the WEIM, please refer to "Chapter 49 Wireless External Interface Module" in the "i.MX25 Multimedia Applications Processor Reference Manual" and "Section 3.7.63 Wireless External Interface Module Timing" in the "i.MX25 Applications Processor for Consumer and Industrial Products" stored in the /document/datasheet directory on the included DVD.

While the timings can be freely changed with WEIM configuration, the delay introduced by the CPLD and buffer in between the CPU (i.MX257) and I/O pins (J1, J2) must be taken into account. Also, care must be taken as the data buffer enable/disable is set with CS3* and CS4*, and the direction switched with RW*.

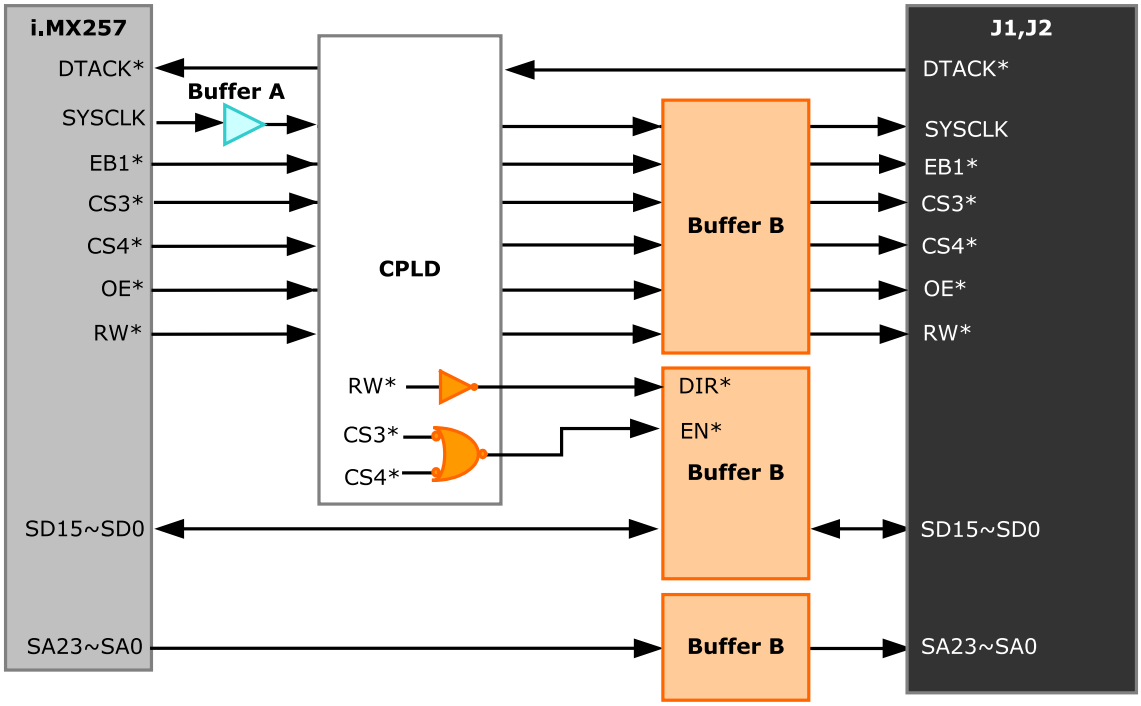


Figure 6.11. Wiring Between CPU and I/O Pins (J1, J2)

The input/output delays introduced by the CPLD and buffers are as shown below.

Table 6.48. Delays Between CPU (i.MX257) and I/O Pins (J1, J2)

Signal Name	Buffer A		CPLD		Buffer B	
	min (ns)	max (ns)	min (ns)	max (ns)	min (ns)	max (ns)
DTACK*	-	-	-	7.6	-	-
SYSCLK	0.7	2.5	-	7.6	1	7.4
EB1*	-	-	-	7.5	1	7.4
CS3*	-	-	-	7.6	1	7.4
CS4*	-	-	-	7.6	1	7.4
OE*	-	-	-	11.9	1	7.4
RW*	-	-	-	11.9	1	7.4
SA	-	-	-	-	1	7.4
SD (CPU to J1, J2)	-	-	-	-	1	7.4

Signal Name	Buffer A		CPLD		Buffer B	
	min (ns)	max (ns)	min (ns)	max (ns)	min (ns)	max (ns)
SD (J1, J2 to CPU)	-	-	-	-	0.7	23.4

Table 6.49. Time Until Buffer Enable/Disable Is Effective

Buffer	From CS3* or CS4* to EN*		CPU to J1, J2		J1, J2 to CPU	
	min (ns)	max (ns)	min (ns)	max (ns)	min (ns)	max (ns)
Enable	-	7.8	0.4	23.7	1.2	12.6
Disable			1.5	29.3	1.7	12

6.3.13.3.2.3. Direct CPU Bus Mode (Synchronous)

Direct CPU Bus Mode (Synchronous) takes on the CS3 (0xB2000000 - 0xB3FFFFFF) memory space. Data widths of 8bit and 16bit can be selected by configuring the Wireless External Interface Module(WEIM). 66MHz is output from SYSCLK, and EB1*, CS3*, and RW* are output synchronously to SYSCLK by the CPLD.

For details on the configuration of the WEIM, please refer to "Chapter 49 Wireless External Interface Module" in the "i.MX25 Multimedia Applications Processor Reference Manual" stored in the /document/datasheet directory on the included DVD.

The CS4 memory space cannot be used in the synchronous direct CPU bus mode.

SYSCLK can be inverted with the Ext Bus Control Register. Also, the access cycle can be lengthened to a maximum of 127 clocks with RDY*. RDY* is input with push-push, and should be kept at a low level when not in use.

EB1* is an Active-Low signal that shows that the data bus (SD15 - SD8) is being use. The lower address bit (SA0) can be used to determine if data bus (SD15 - SD8) is being used or not. The relationship between data access, EB1* and SA0 is shown in Table 6.50, “EB1*, SA0 and Data Access Relationship”.

Please note that while data bus (SD7 to SD0) is used for lower 8bit read accesses, EB1* will have a low level.

Table 6.50. EB1*, SA0 and Data Access Relationship

Data	Access	EB1*	SA0
16bit (SD15 - SD0)	Read	Low	Low
	Write		
Higher 8bit (SD15 - SD8)	Read	Low	High
	Write		
Lower 8bit (SD7 - SD0)	Read	Low	Low
	Write	High	

Input signal timings are as shown below.

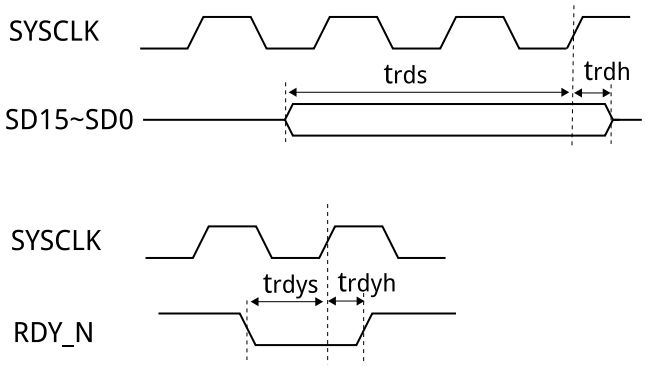


Figure 6.12. Input Signal Timings

Table 6.51. Input Signal Timings

Symbol	Explanation	min (ns)	max (ns)
t_{rds}	SD15 - SD0 setup time for clock	31.4	-
t_{rdh}	SD15 - SD0 hold time for clock	0	-
t_{rdys}	RDY* setup time for clock	8.7	-
t_{rdyh}	RDY* hold time for clock	0	-

Output signal timing is as shown below.

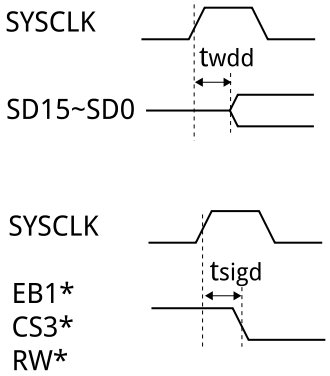


Figure 6.13. Output Signal Timings

Table 6.52. Output Signal Timings

Symbol	Explanation	min (ns)	max (ns)
t_{wdd}	SD15 - SD0 delay for clock	-	9.2
t_{sigd}	EB1*, CS3* and RW* delay for clock	-	9

An example of read bus access timing when using RDY* is shown below.

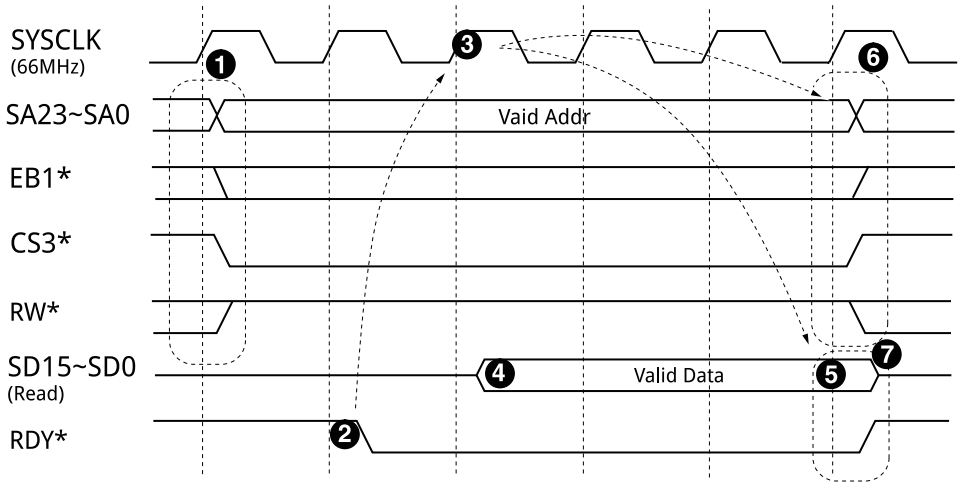


Figure 6.14. Direct CPU Bus Mode (Synchronous) Read Bus Access Timing When Using RDY*

1. CPU: outputs valid address on SA23 - SA0, asserts CS3* and EB1* (when data width is 16bit)
2. Device: latches address, asserts RDY* once ready for data output
3. CPU: detects RDY* assert on clock risking edge
4. Device: outputs valid data on SD15 - SD0
5. CPU: latches data on rising edge three clocks after RDY* assert
6. CPU: deasserts all signals
7. Device: stops valid data output, deasserts RDY*

An example of write bus access timing when using RDY* is shown below.

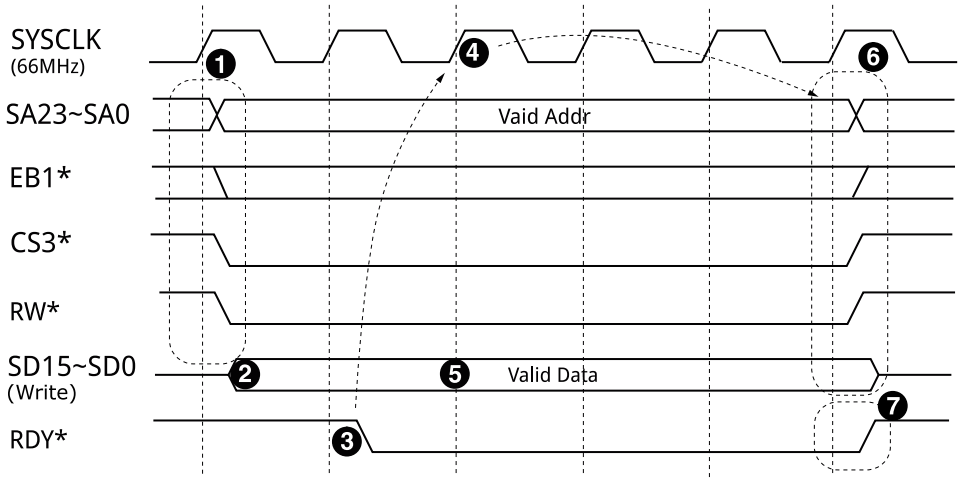


Figure 6.15. Direct CPU Bus Mode (Synchronous) Write Bus Access Timing When Using RDY*

1. CPU: outputs valid address on SA23 - SA0, asserts CS3*, RW* and EB1* (when using SD15 - SD7)
2. CPU: outputs valid data on SD15 - SD0
3. Device: latches address, asserts RDY* once ready for data input
4. CPU: detects RDY* assert on clock risking edge

❺ Device: reads data

❻ CPU: deasserts all signals three clocks after RDY* assert

❼ Device: deasserts RDY*

The cycle completes in 4 clocks if RDY* is not used.

6.3.14. LED1, LED2 (LAN LEDs) - Armadillo-460

LED1 and LED2 are the LAN interface status LEDs. They are shown on the upper part of CON2.

Table 6.53. LAN LED Meanings - Armadillo-460

LED	Name (color)	On	Off
LED1	Link LED (green)	A LAN cable is connected and a 10BASE-T or 100BASE-TX link has been established.	A LAN cable is not connected or the LAN status of the connected device is not active.
LED2	Activity LED (yellow)	Data transmit/receive	No data

6.3.15. LED3, LED4, LED5 (User LEDs) - Armadillo-460

LED3, LED4 and LED5 are LEDs which can be used freely by the user. These LEDs can be controlled once the i.MX257 signals they are connected to are set to GPIO output mode.

Table 6.54. User LED Function - Armadillo-460

LED	Name (color)	Function
LED3	User LED (red)	Connected to NFALE (GPIO3_28) pin on i.MX257 (low: off, high: on)
LED4	User LED (green)	Connected to NFCLE (GPIO3_29) pin on i.MX257 (low: off, high: on)
LED5	User LED (yellow)	Connected to BOOT_MODE0 (GPIO4_30) pin on i.MX257 (low: off, high: on)

LED5 is connected to the same signal as JP1. LED5 cannot be controlled while JP1 is shorted.

6.3.16. SW1, SW3, CON22 (User Switches) - Armadillo-460

SW1 is a switch which can be freely used by the user and is connected to GPIO3_30 on the i.MX257. The switch status can be obtained once the i.MX257 signal it is connected to is set to GPIO input mode. SW3 and CON22 share the same signal as SW1 on Armadillo-460.

Table 6.55. User Switch Function - Armadillo-460

SW	Function
SW1, SW3	Connected to NFWP_B (GPIO3_30) pin on i.MX257 (low: switch pressed, high: switch not pressed)

Table 6.56. CON22 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	SW1	In/Out	User switch signal
2	GND	Power	Power (GND)

Pin Number	Signal Name	I/O	Function
3	JP1PU	Out	390Ω pull-up by 3.3V_CPU, signal line shared with JP1 (pin 2)
4	JP1	In	Connected to BOOT_MODE0 (GPIO4_30) pin on i.MX257 (10kΩ pull-down), shared with JP1 (pin 1)
5	JP2	In	Connected to NFC_CE0 (GPIO3_22) pin on i.MX257 (10kΩ pull-up by 3.3V_CPU), signal line shared with JP2 (pin 2)
6	GND	Power	Power (GND)

6.3.17. JP1 (Boot Mode Configuration Jumper) - Armadillo-460

The JP1 jumper is used to configure the board's boot mode. The boot mode is determined at power on time according to the jumper state.

Table 6.57. Boot Mode Configuration Jumper States - Armadillo-460

JP1	Behavior
Open	On-board flash memory boot
Shorted	UART boot: UART2 (CON3 or CON4)

Table 6.58. JP1 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	JP1	In	Connected to BOOT_MODE0 (GPIO4_30) pin on i.MX257 (10kΩ pull-down), shared with CON22 (pin 4)
2	JP1PU	Out	390Ω pull-up by 3.3V_CPU, signal line shared with CON22 (pin 3)

JP1 is connected to the same signal as LED5. Please do not use JP1 in a shorted state after booting to on-board flash memory.

6.3.18. JP2 (User Jumper) - Armadillo-460

The JP2 jumper can be used freely by the user. The jumper status can be obtained once the i.MX257 signal it is connected to is set to GPIO input mode.

Table 6.59. User Jumper Function - Armadillo-460

JP	Function
JP2	Connected to NF_CE0 (GPIO3_22) on i.MX257 (low: shorted, high: open)

Table 6.60. JP2 Signals - Armadillo-460

Pin Number	Signal Name	I/O	Function
1	GND	Power	Power (GND)
2	JP2	In	Connected to NFC_CE0 (GPIO3_22) pin on i.MX257 (10kΩ pull-up by 3.3V_CPU), signal line shared with CON22 (pin 5)

6.3.19. On-Board Real-Time Clock - Armadillo-460

Armadillo-460 is equipped with a Seiko Instruments real-time clock (RTC). The RTC will continue to operate from a laminated ceramic capacitor for a few minutes after power has been cut. It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

The main specifications of the RTC are as follows.

Table 6.61. RTC Specifications - Armadillo-460

Real-Time Clock (RTC)	Seiko Instruments RTC (S-35390A)
Backup	300sec (typ.), 60sec (min.) External battery can be connected via the RTC External Backup Power Connector (CON20)
Power Supply Voltage	DC2.0 - 3.5V

The power supply makeup of the on-board real-time clock is shown in Figure 6.16, “On-Board Real-Time Clock Power Supply Makeup - Armadillo-460”. The Armadillo-460 internal power supply (+3.3V_CPU), CON13 and CON20 are connected to the on-board real-time clock, and an external battery can be connected to CON13 and CON20.

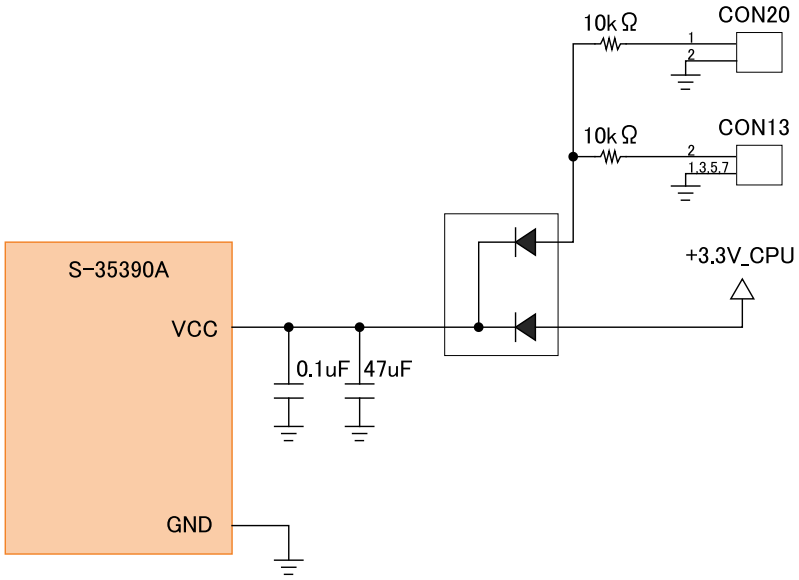


Figure 6.16. On-Board Real-Time Clock Power Supply Makeup - Armadillo-460

The time accuracy of the RTC is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

As the backup time of the RTC is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

6.3.19.1. On-Board Real-Time Clock Makeup - Armadillo-460

The RTC Control Register in the CPLD controls the RTC data (RTC_SDA) and clock (RTC_SCL). The CPLD pins connected to the RTC are three-state buffer outputs. They output a low level signal when the RTC Control Register is set to '0', and when the register is set to '1' they go into a high impedance state allowing them to accept input.

For information on the CPLD memory map and registers, please refer to Appendix E, CPLD Registers - Armadillo-460.

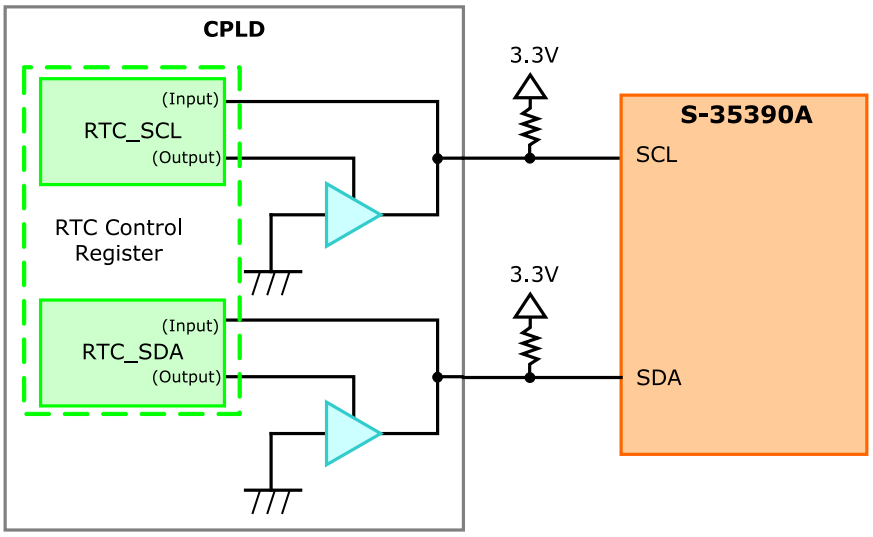


Figure 6.17. On-Board Real-Time Clock and CPLD Connection - Armadillo-460

Chapter 7. Design Information

7.1. Reference Circuits

7.1.1. GPIO

Reference circuits for when CON9, CON11 (Armadillo-440/460 only) and CON14 signals are used as GPIO are shown in Figure 7.1, “GPIO Reference Circuits”.

The operation of the reference circuits is not guaranteed in any form. When applying the circuits, please ensure to choose appropriate values after carrying out a thorough evaluation.

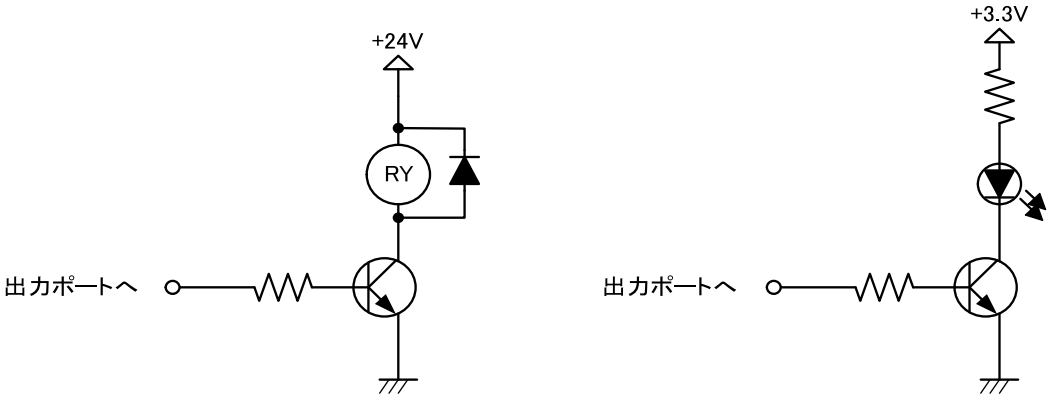


Figure 7.1. GPIO Reference Circuits

7.1.2. Keypad

A reference circuit for when using the CON11 keypad signals is shown in Figure 7.2, “Keypad Signals Reference Circuit”.

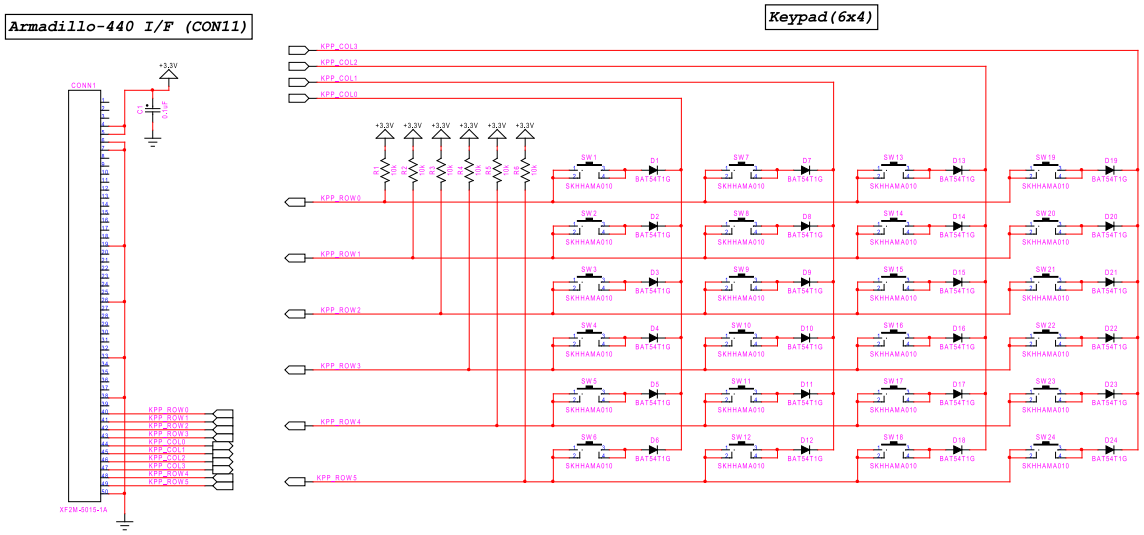


Figure 7.2. Keypad Signals Reference Circuit

7.1.3. CAN

A reference circuit[1] for when using the CON9 CAN2 signals[2] is shown in Figure 7.3, “CAN Signals Reference Circuit”.

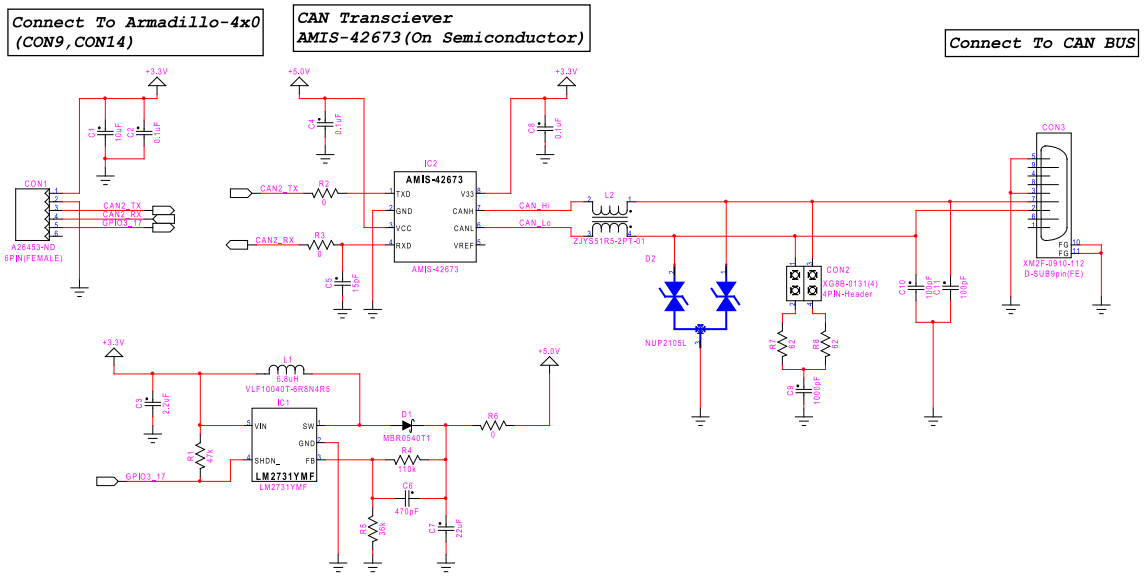


Figure 7.3. CAN Signals Reference Circuit

7.1.4. Direct CPU Bus Mode Compatible Expansion Board Reference Code Example

The VHDL sample code shown below selects the direct CPU bus mode (synchronous), sets the data bus width to 16bit and performs read/write access of J1/J2 (Armadillo-460).

```
library IEEE;
use ieee.std_logic_1164.all;
```

[1]GPIO3_17 on CON9 which is adjacent to CON14 on Armadillo-4x0 is used for the GPIO of CON1 in the reference circuits.
[2]The same circuit applies when using the CAN1 signals on CON11.

```
entity direct_sync is
    generic (
        C_AWIDTH    : integer := 24;
        C_DWIDTH    : integer := 16;
        C_BASEADDR  : std_logic_vector := x"B2000000";
        C_HIGHADDR  : std_logic_vector := x"B27FFFFF"
    );
    port (
        SYSCLK      : in    std_logic;                      -- Clock
        RESET       : in    std_logic;                      -- Reset
        SA          : in    std_logic_vector(C_AWIDTH-1 downto 0);  --Address
        CS3_N       : in    std_logic;                      -- Chip Select3
        EB1_N       : in    std_logic;                      -- Enable Byte(15:8)
        RW_N        : in    std_logic;                      -- Read Write
        RDY_N       : out   std_logic;                      -- Ready
        SD          : inout std_logic_vector(C_DWIDTH-1 downto 0)  -- Data
    );
end direct_sync;

architecture Behavioral of direct_sync is

signal reg0     : std_logic_vector(C_DWIDTH-1 downto 0);    -- Register
signal data_o   : std_logic_vector(C_DWIDTH-1 downto 0);    -- Output Data
signal RDY_d1   : std_logic;                                -- RDY Delay
signal RDY_N_w  : std_logic;                                -- RDY wire
signal EB0_N    : std_logic;                                -- Enable Byte(7:0)

begin

    EB0_N <= SA(0);

-------------------
-- RDY Signal Gen
-------------------
    process(SYSCLK, RESET)
    begin
        if RESET = '1' then
            RDY_d1 <= '1';
            RDY_N_w <= '1';
        elsif SYSCLK'event and SYSCLK = '1' then
            RDY_d1 <= CS3_N;
            RDY_N_w <= RDY_d1;
        end if;
    end process;

    RDY_N <= RDY_N_w;

------------------
-- Write Access
------------------
    process(SYSCLK, RESET)
    begin
        if RESET = '1' then
            reg0 <= (others => '0');
        elsif SYSCLK'event and SYSCLK = '1' then
            if CS3_N = '0' and RW_N = '0' and RDY_N_w = '0' then
                case SA(3 downto 1) is
```

```
                    when "000" =>
                        if EB1_N = '0' then
                            if EB0_N = '0' then
                                reg0 <= SD;
                            else
                                reg0(15 downto 8) <= SD(15 downto 8);
                            end if;
                        else
                            reg0(7 downto 0) <= SD(7 downto 0);
                        end if;
                    when others => null;
                end case;
            end if;
        end if;
    end process;

------------------
-- Read Access
------------------
    process(SYSCLK, RESET)
    begin
        if RESET = '1' then
            data_o <= (others => '0');
        elsif SYSCLK'event and SYSCLK = '1' then
            if CS3_N = '0' and RW_N = '1' and RDY_N_w = '0' then
                case SA(3 downto 1) is
                    when "000" => data_o <= reg0;
                    when others => data_o <= (others => '0');
                end case;
            end if;
        end if;
    end process;

    SD <= data_o when CS3_N = '0' and RW_N = '1' and RDY_N_w = '0' else (others =>
'Z');

end Behavioral;
```

Figure 7.4. Direct CPU Bus Mode (Synchronous) Reference Access Example

7.2. Towards Productization

7.2.1. Radiated Noise

The following is information on how to reduce radiated noise from the Armadillo-400 Series boards when they are installed in a case as part of productization.

To decrease the amount of radiated noise when using Armadillo-440 or Armadillo-460 with the Armadillo-400 Series LCD Expansion Board, strengthening the ground outside of the flexible flat cable (FFC) GND is effective. For example, by connecting the fixing holes of the Armadillo-440 or Armadillo-460 and the LCD Expansion Board with a wide conducting line, connecting them to a metal enclosure with a wide conducting line or grounding the metal enclosure.

Armadillo-460 in both PC/104 Expansion Bus Compatibility Mode and Direct CPU Bus Mode has cleared Class A as defined under VCCI Council standards. In Direct CPU Bus Mode, there is a possibility that more radiated noise will be produced from the board than in PC/104 Expansion Bus Compatibility Mode. To reduce radiated noise produced from the Armadillo-460 board in Direct CPU Bus Mode, appropriately connecting terminating resistors between GND and the unused SYSCLK, address and data lines is effective.

Please be aware of the following points when newly designing an expansion board which connects to the LCD interface on Armadillo-440 and Armadillo-460.

With an expansion board that includes a device that has large power use fluctuations, such as with an audio amp, when only the GND line of the flexible flat cable (FCC) is connected the expansion board may produce electromagnetic noise. To mitigate the noise, strengthening of the expansion board's ground is recommended. For example, by connecting the fixing holes of the Armadillo-440 or Armadillo-460 and expansion board by metal plate or wide conducting line or grounding the metal enclosure.

7.2.2. ESD

The following is information on how to improve the ESD tolerance of the Armadillo-400 Series boards when they are installed in a case as part of productization.

To improve ESD tolerance on the Armadillo-400 Series boards, strengthening the ground is effective. For example, connecting the board ground and metal enclosure with a wide conducting line, or grounding the metal enclosure.

To improve ESD tolerance when using Armadillo-440 or Armadillo-460 with the Armadillo-400 Series LCD Expansion Board, strengthening the ground outside of just the flexible flat cable (FFC) GND is effective. For example, by connecting the fixing holes of the Armadillo-440 or Armadillo-460 and the LCD Expansion Board with a wide conducting line, connecting them to a metal enclosure with a wide conducting line or grounding the metal enclosure.

When connecting Armadillo-460 to a device via the included D-sub9 / 10 pin serial conversion cable, it is possible that ESD tolerance will not clear Contact:±2kV (JIS C 61000-4-2 : Level 1). If the ground of the D-sub9 / 10 pin serial conversion cable

is connected to the ground of the Armadillo-460 board by a wide conducting line, it can be expected to clear Contact: ±4kV (JIS C 61000-4-2 : Level 2)

Please be aware of the following points when newly designing a PC/104 expansion board which connects to the expansion bus interface on Armadillo-460.

The ESD tolerance of Armadillo-460 with a PC/104 expansion board connected clears Contact: ±2kV (JIS C 61000-4-2 : Level 1). If the PC/104 expansion board is designed so that its fixing holes are GND and the fixing holes of both the PC/104 expansion board and Armadillo-460 are connected by a wide conducting line, it can be expected to clear Contact: ±4kV (JIS C 61000-4-2 : Level 2)

Chapter 8. Board Outline Diagrams

8.1. Armadillo-420 Board Outline Diagrams

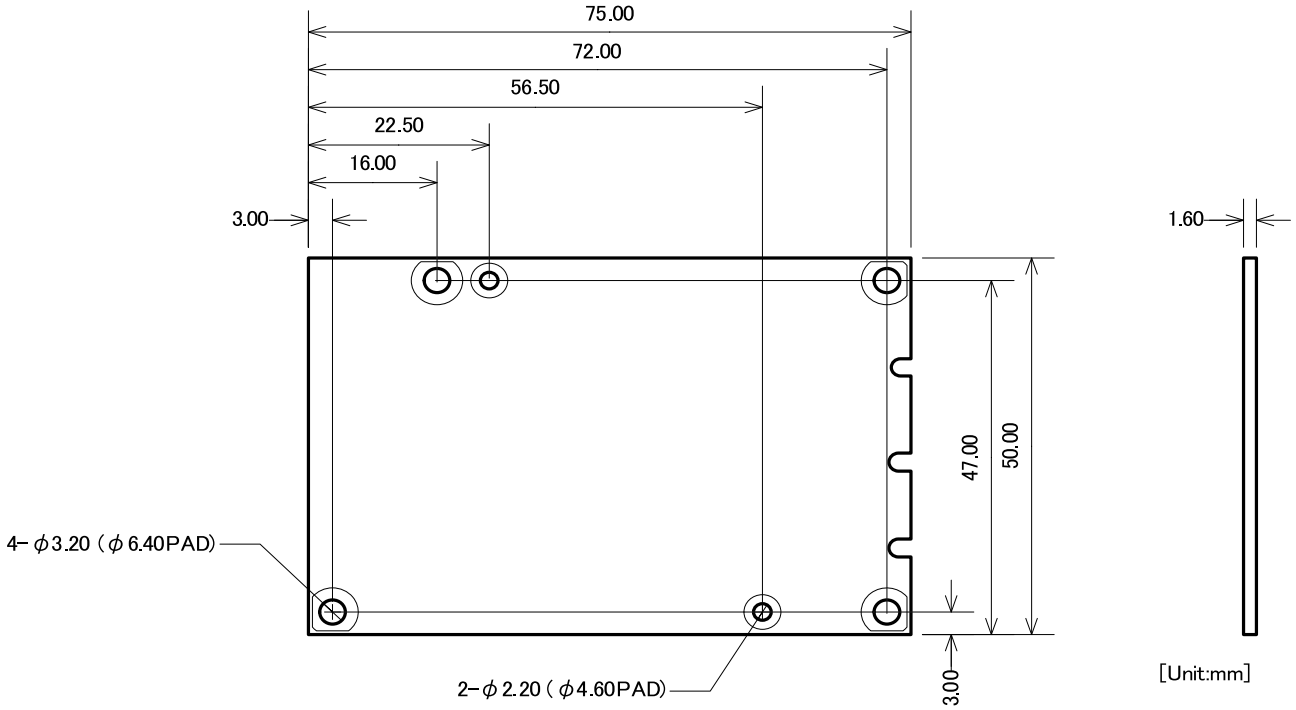


Figure 8.1. Armadillo-420 Board Outline and Fixing Hole Measurements

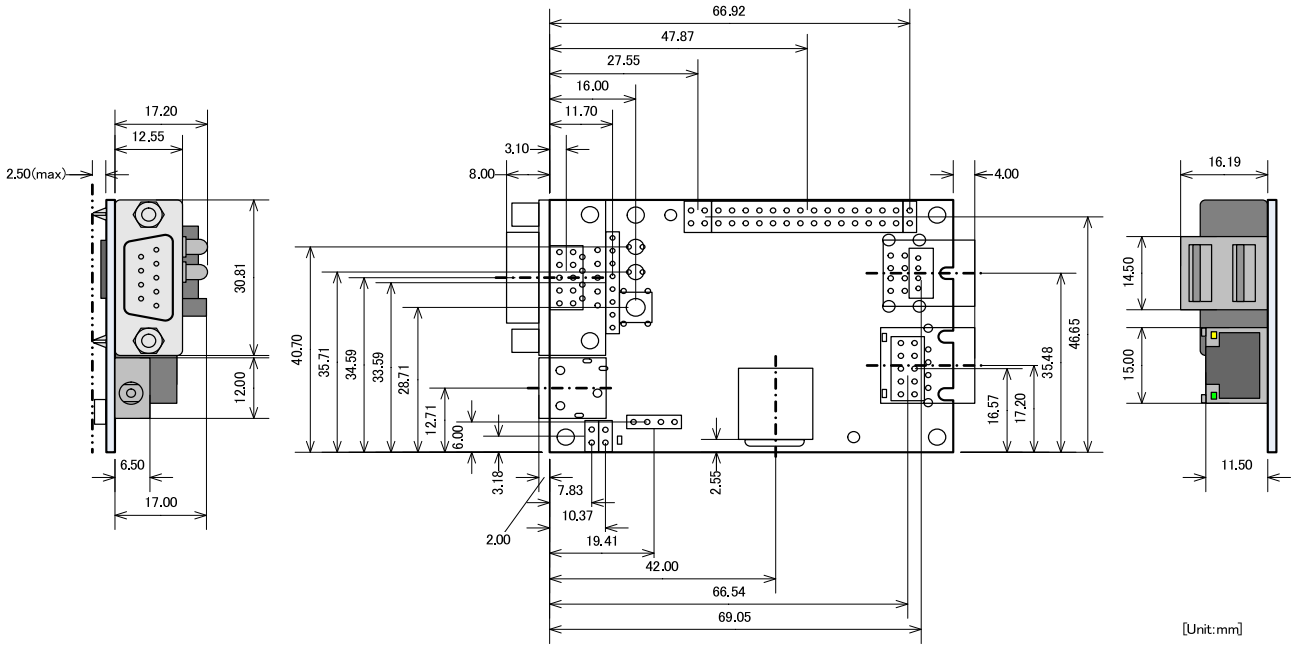


Figure 8.2. Armadillo-420 Connector Center Measurements

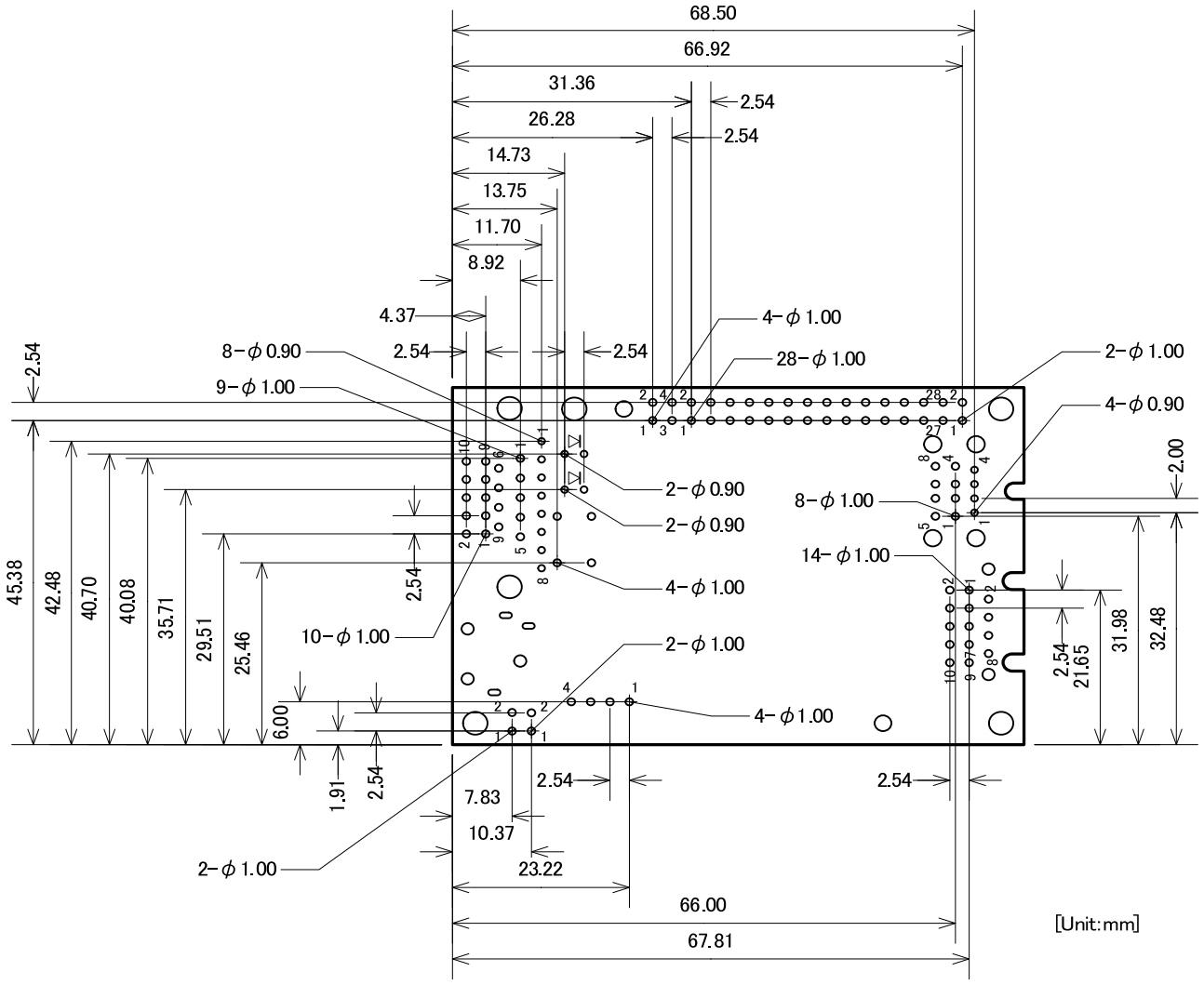


Figure 8.3. Armadillo-420 Connector Hole Measurements

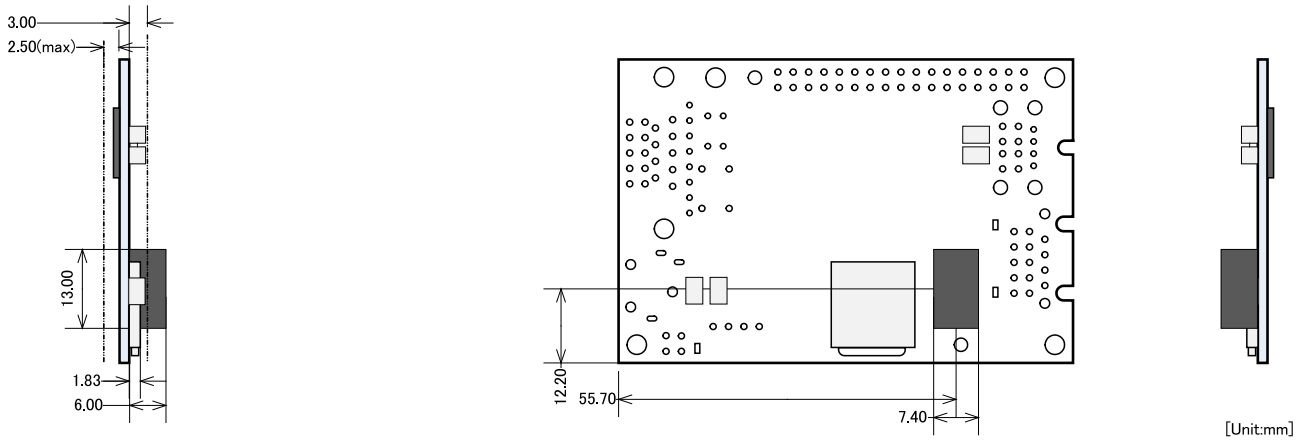


Figure 8.4. Armadillo-420 Mass Production Board Component Placement

8.2. Armadillo-440 Board Outline Diagrams

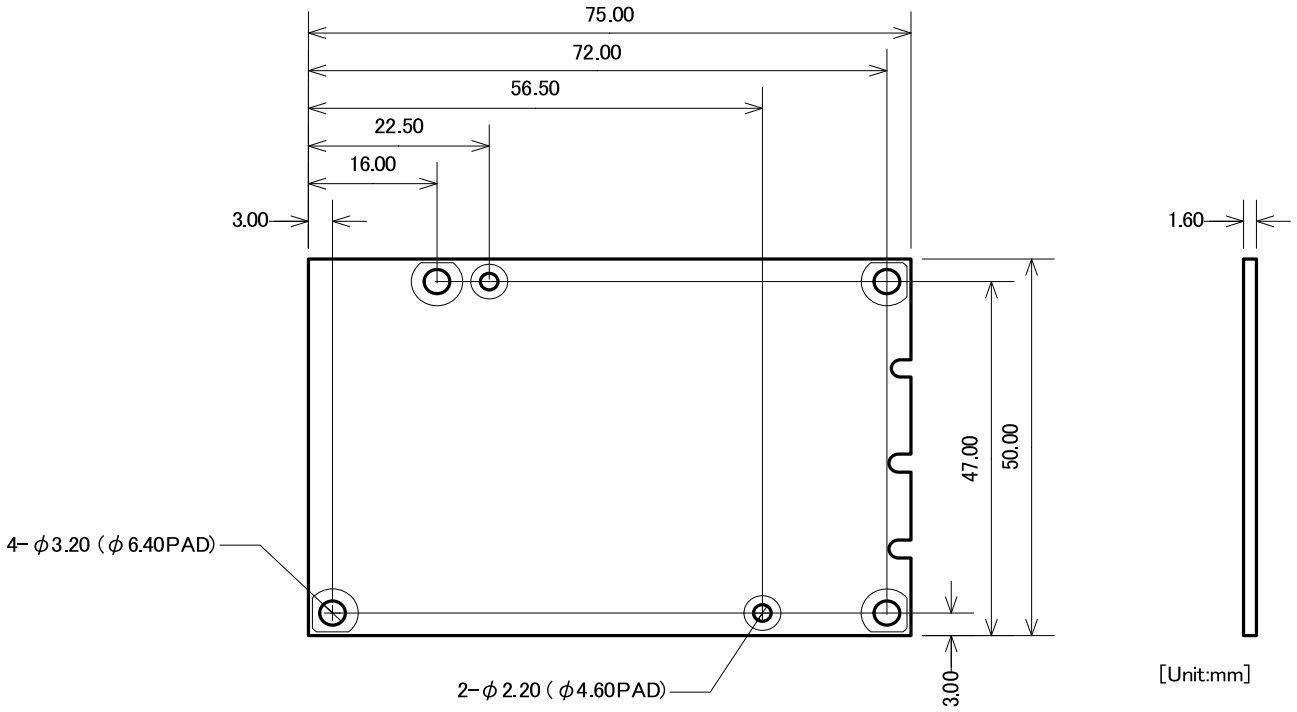


Figure 8.5. Armadillo-440 Board Outline and Fixing Hole Measurements

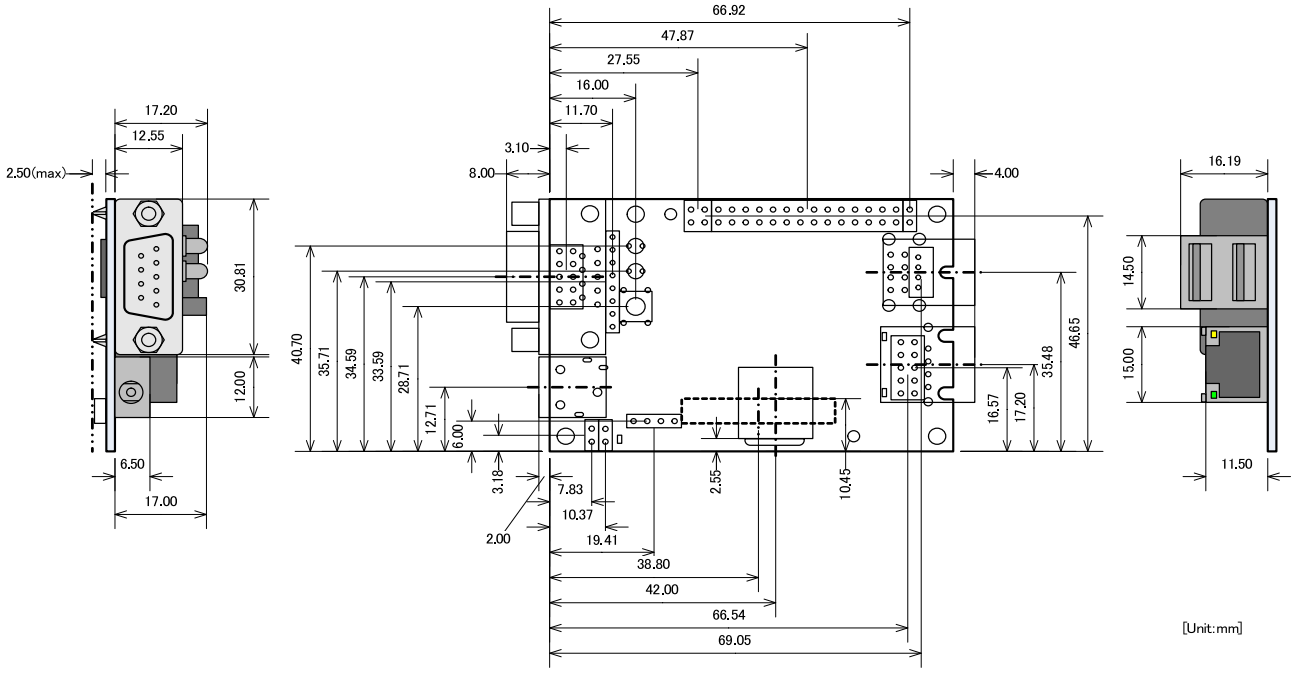


Figure 8.6. Armadillo-440 Connector Center Measurements

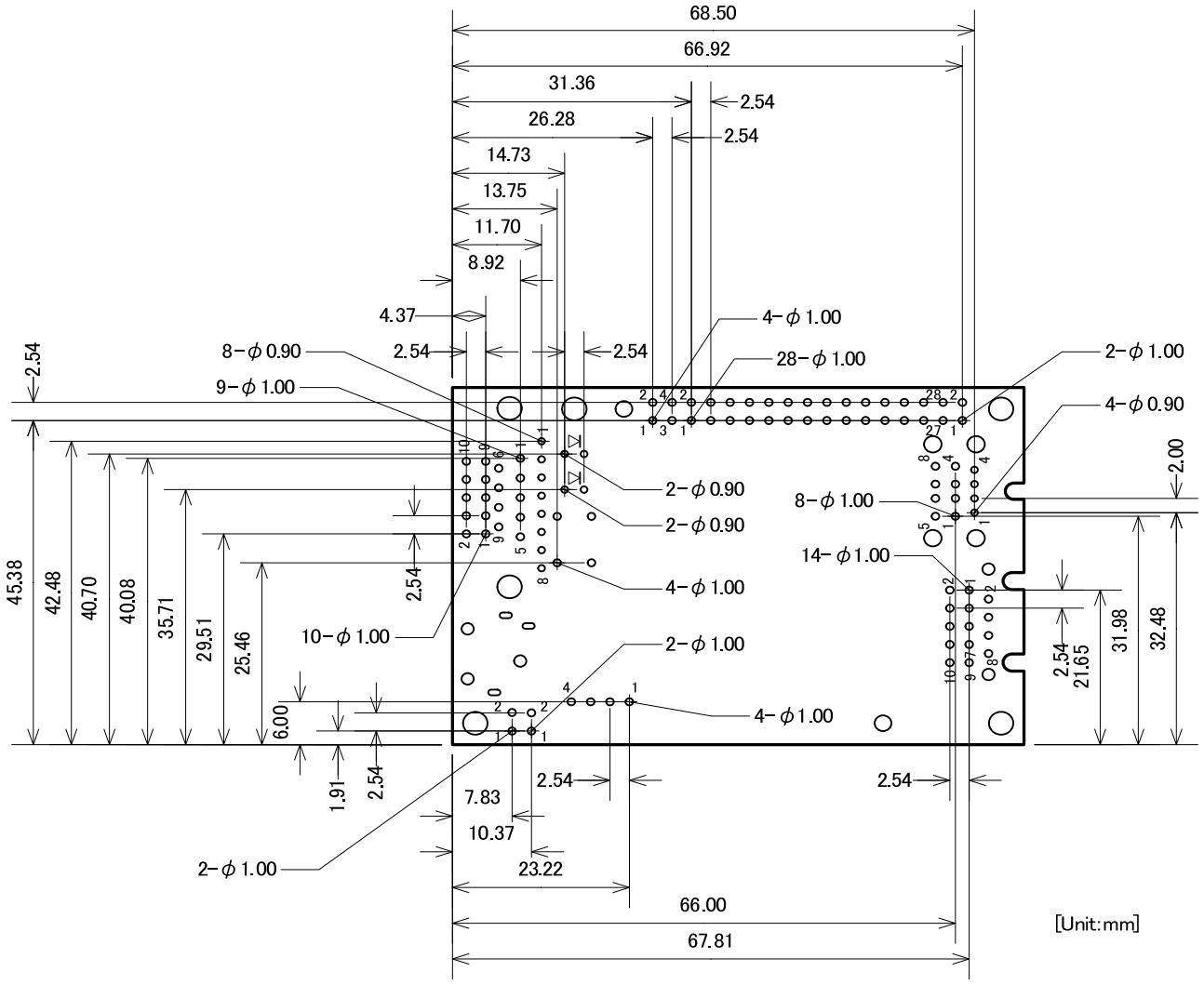


Figure 8.7. Armadillo-440 Connector Hole Measurements

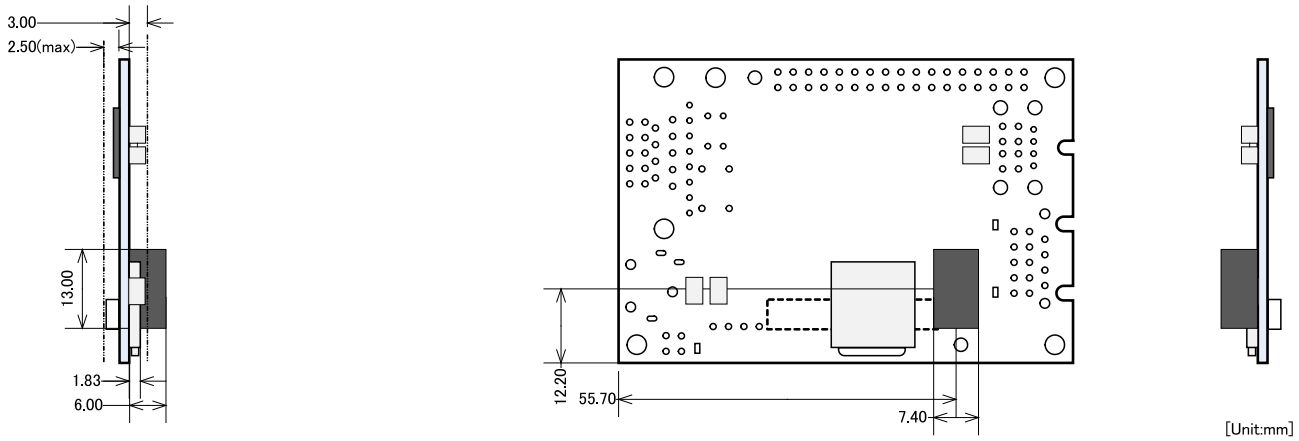


Figure 8.8. Armadillo-440 Mass Production Board Component Placement

8.3. Armadillo-460 Board Outline Diagrams

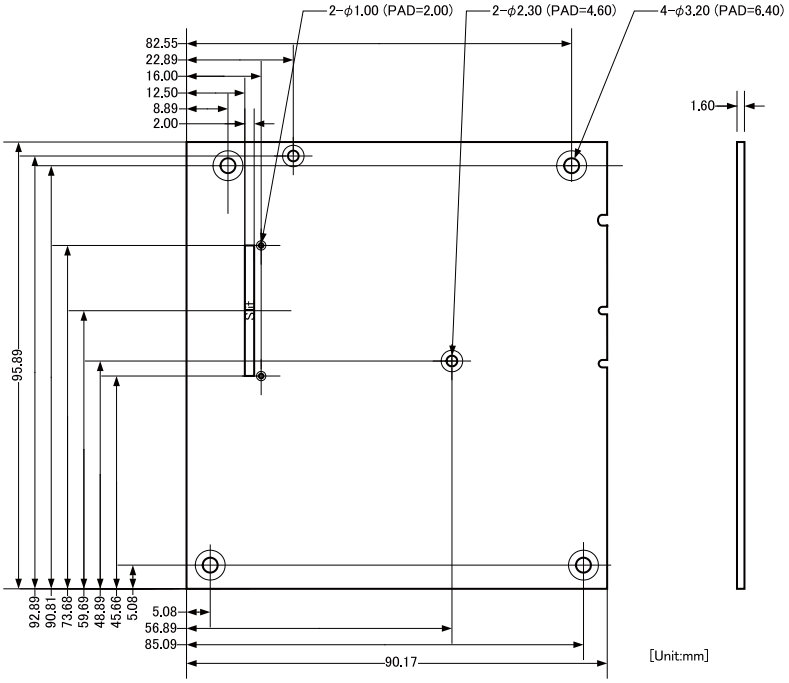


Figure 8.9. Armadillo-460 Board Outline and Fixing Hole Measurements

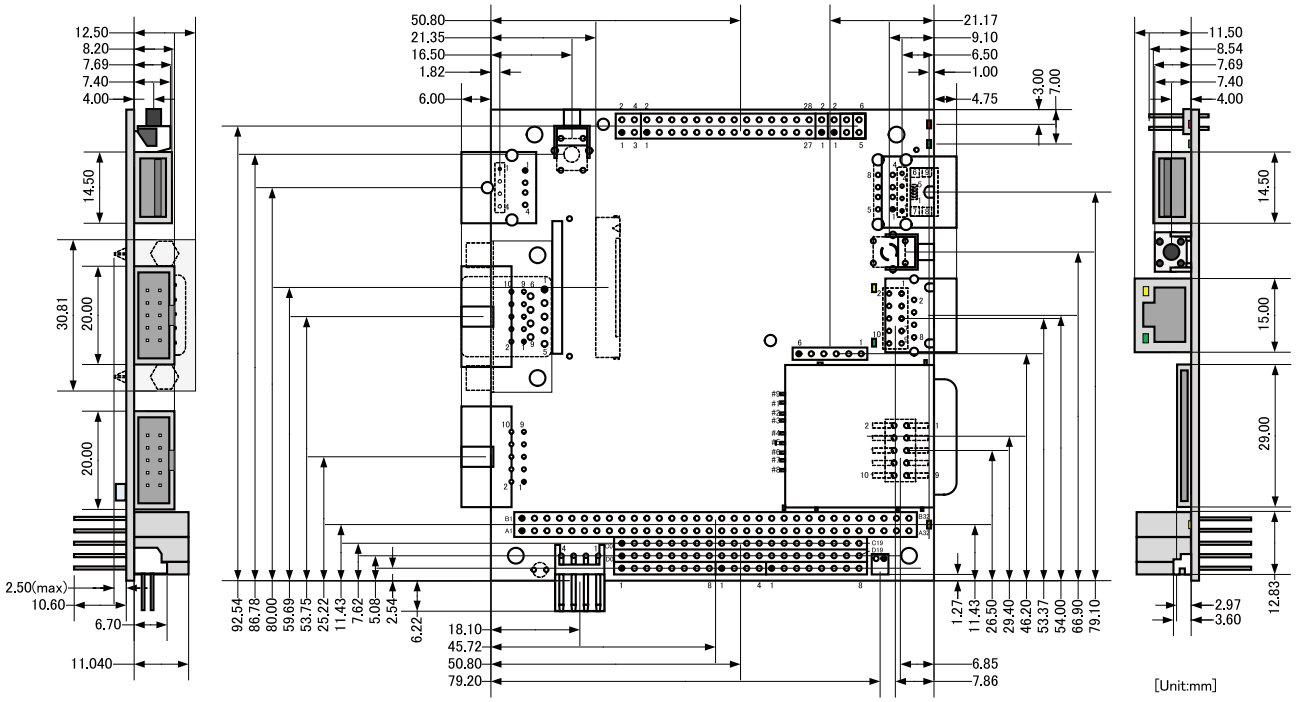


Figure 8.10. Armadillo-460 Connector Center Measurements

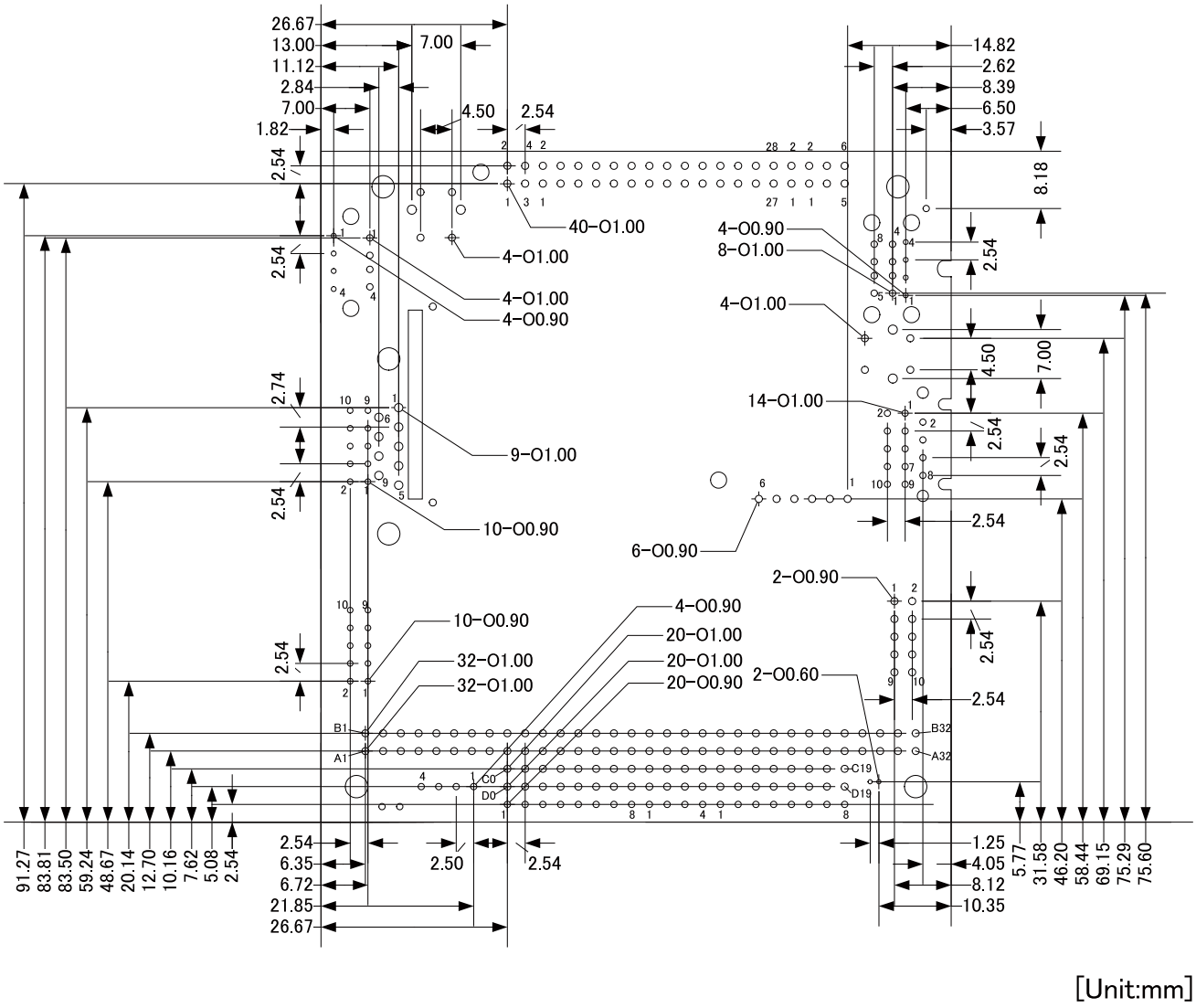


Figure 8.11. Armadillo-460 Connector Hole Measurements

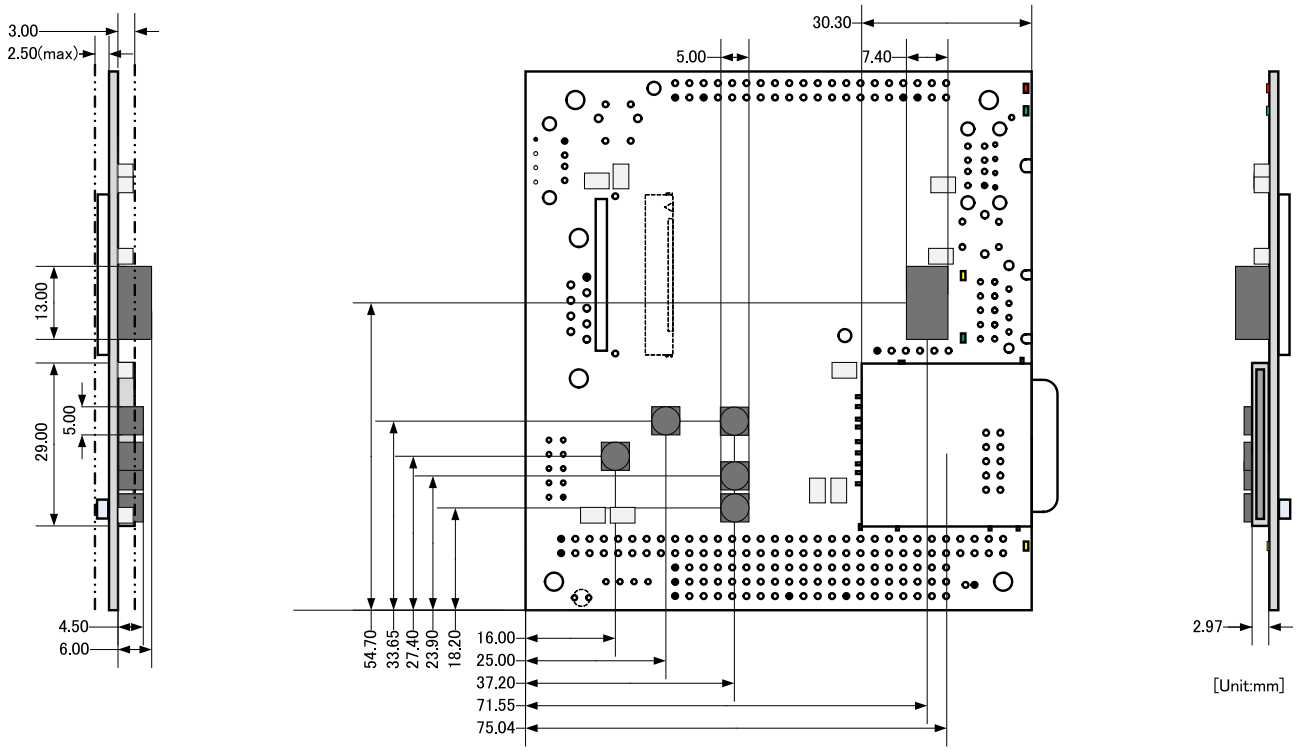


Figure 8.12. Armadillo-460 Mass Production Board Component Placement

Chapter 9. Expansion Boards / Option Modules

The following provides hardware details of the expansion boards and option modules which can be connected to the Armadillo-400 series.

9.1. Armadillo-400 Series LCD Expansion Board

The Armadillo-400 Series LCD Expansion Board (product revision B) is included in the Armadillo-400 Series LCD Option Set (Product ID: OP-A400-LCD43EXT-L01).

9.1.1. Board Overview

The Armadillo-400 Series LCD Expansion Board (hereafter LCD Expansion Board) connects to the LCD expansion interface (CON11) on the Armadillo-400 Series and includes a touch-screen LCD module, audio codec and real-time clock (hereafter RTC). The main specifications of the LCD Expansion Board and the LCD module itself are as follows.

Please note that some specifications differ between the different product revisions of the LCD Expansion Board. For information on determining the product revision, please refer to the "Armadillo-400 Series Revision Information" on the Armadillo Site product manual page.

Table 9.1. LCD Expansion Board Specifications

LCD I/F	Data Image, Inc LCD (FG040360DSSWBG03) connector General purpose LCD I/F connector x1 Back-light LED driver	
Audio	Wolfson codec (WM8978GEFL/V) Stereo headphone output jack x1 Mono mic input jack x1	
Real-Time Clock (RTC)	Seiko Instruments RTC (S-35390A)	
RTC Backup	Product Revision A	Approximately 5 days (environmental temperature of 25℃, reference value)
	Product Revision B	300sec (typ.), 60sec (min.), external battery can be connected via External RTC Backup Connectors (CON8, CON9, CON102)
LED / Switch	Tact Switch x 3 Power LED (green) x1	
Board Size	106.0 × 82.0 mm (not including protrusions)	
Power Supply Voltage	Product Revision A	Main power: DC3.1 - 3.3V LCD back-light: DC2.8 - 5.5V
	Product Revision B	Main power: DC3.3V±0.2V LCD back-light: DC2.8 - 5.5V
Power Consumption	Approx. 0.8W (including LCD module)	
Operating Temperature	Product Revision A	-10 - 60℃ (with no condensation)
	Product Revision B	-20 - 70℃ (with no condensation)

The time accuracy of the RTC is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

As the backup time of the RTC is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

The RTC backup electric double-layer capacitor (Panasonic EECEN0F204RK) equipped on the LCD Expansion Board (Product Revision A) has a finite lifetime. Its capacity diminishes over time while its internal resistance increases.

The "10℃ Double Rule" can generally be applied for the lifetime estimate of electric double-layer capacitors.

$$Lx = Lo \times 2^{((To-Tx)/10)}$$

Here, Lo is guaranteed lifetime (hours) at the maximum temperature, Lx is estimated lifetime (hours) of actual use, To is the maximum temperature (℃), and Tx is the actual use environmental temperature (℃).

The guaranteed durability values published by the maker for EECEN0F204RK are 500 hours at +60℃ (capacitance change within ±30% of original, internal resistance less than 4kΩ). Supposing the environmental temperature was 25℃, the estimated lifetime would be as follows.

$$Tx = 500 \times 2^{((60-25)/10)} = 5600 \text{ hours approx.}$$

Note that as the lifetime of electric double-layer capacitors is effected by the length of time voltage is applied and not the number of charge cycles, the time calculated above is the cumulative operating time.

If the prescribed lifetime is exceeded, abrupt characteristic degradation and liquid leaking may occur. If using in mass produced products where long term continuous operation is expected, please carry out regular inspections and replacements.

Table 9.2. LCD Module Specifications

Type	FG040360DSSWBG03
Maker	Data Image, Inc
Type	TFT
Colors	24bit
Screen Size	4.3 inch
Backlight	LED (VL=15 - 18V, IL=40mA)
Touch Panel	4-Wire Resistive

Dimensions	105.5(W) x 67.2(H) x 4.2(D) mm
Active Area	95.04(W) x 53.856(H) mm
Dot Pattern	480 x (R, G, B) x 272 dots
Dot Pitch	0.066(W) x 0.198(H) mm
Operating Temperature	-20 - 70℃

The touch panel LCD module included in the LCD Model Development Set for evaluation and development is fixed with flexible double sided tape. If a strong force is applied to the LCD screen the double sided tape may give and the LCD frame may touch the board wiring. Please take care not to push the LCD screen stronger than necessary.

It is recommended to fix the LCD module in place with a metal fitting like that shown in Figure 9.8, “LCD Metal Fittings Assembly Example for LCD Expansion Board (Product Revision B)” for mass produced products.

9.1.2. Interface Layout

9.1.2.1. LCD Expansion Board (Product Revision A)

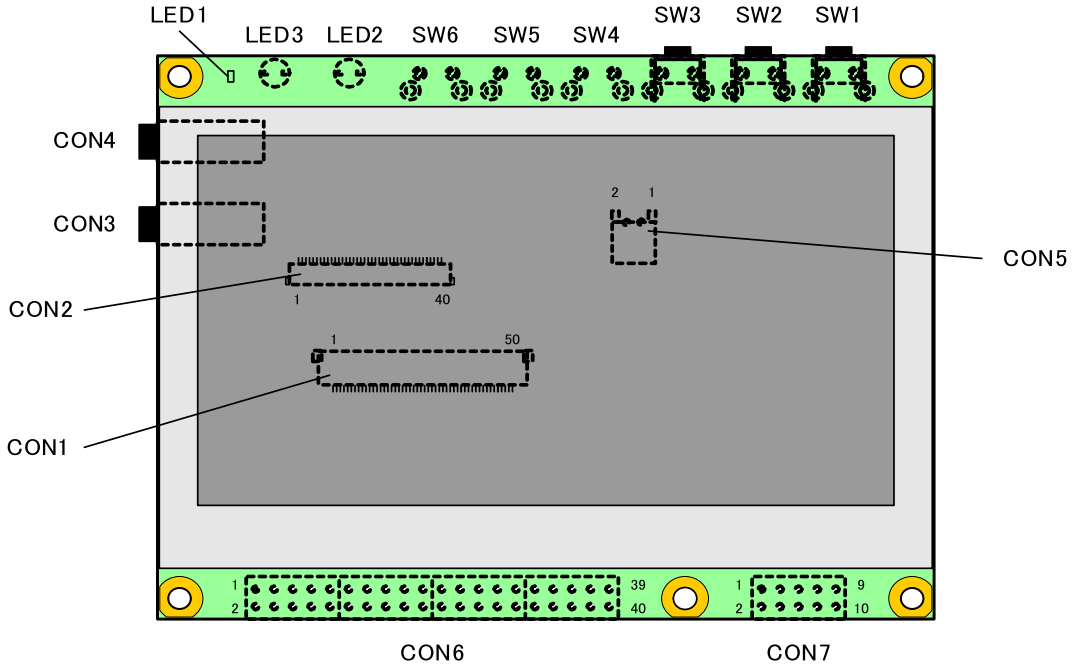


Figure 9.1. LCD Expansion Board (Product Revision A) Interface Layout

Table 9.3. LCD Expansion Board (Product Revision A) Interface Details

Part Number	Interface	Shape	Notes
CON1	Armadillo-400 Series connection	FFC Connector (50P) (0.5mm pitch)	
CON2	Data Image LCD	FFC Connector (40P) (0.5mm pitch)	
CON3	Mic in	Mini jack (ϕ3.5mm)	
CON4	Headphone out	Mini jack (ϕ3.5mm)	

Part Number	Interface	Shape	Notes
CON5	Reserve terminal	Pin headers (2P) (2mm pitch)	Connector not mounted
CON6	General Purpose LCD	Pin headers (40P) (2.54mm pitch)	Connector not mounted
CON7	Reserve terminal	Pin headers (10P) (2.54mm pitch)	Connector not mounted
SW1, SW2, SW3	User switch	Tact switch	
SW4, SW5, SW6	User switch	Tact switch	Switch not mounted
LED1	Power LED	LED (green, surface mount)	
LED2, LED3	User LED	LED (ϕ3mm)	LED not mounted

For the signals of each connector on the LCD Expansion Board, please refer to the "Armadillo-400 Series LCD Expansion Board Circuit Diagram" stored in the /document/hardware directory on the included DVD.

As CON2 and CON6 on the LCD Expansion Board are connected to the same signal lines they cannot be used at the same time. Please disconnect the Data Image LCD from CON2 when connecting another LCD module to CON6.

9.1.2.2. LCD Expansion Board (Product Revision B)

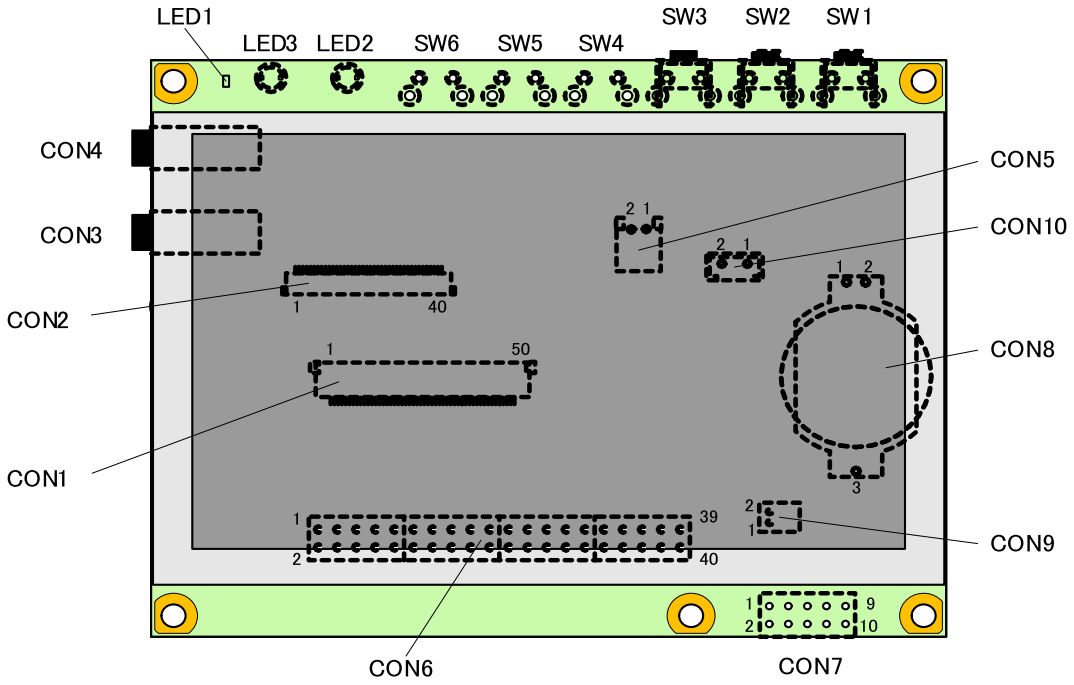


Figure 9.2. LCD Expansion Board (Product Revision B) Interface Layout

Table 9.4. LCD Expansion Board (Product Revision B) Interface Details

Part Number	Interface	Shape	Notes
CON1	Armadillo-400 Series connection	FFC Connector (50P) (0.5mm pitch)	
CON2	Data Image LCD	FFC Connector (40P) (0.5mm pitch)	
CON3	Mic in	Mini jack (ϕ3.5mm)	
CON4	Headphone out	Mini jack (ϕ3.5mm)	
CON5	Reserve terminal	Pin headers (2P) (2mm pitch)	Connector not mounted
CON6	General Purpose LCD	Pin headers (40P) (2.54mm pitch)	Connector not mounted
CON7	Reserve terminal	Pin headers (10P) (2.54mm pitch)	Connector not mounted
CON8	RTC External Backup Power In 1[a]	Battery holder HU2032 (Takachi Electronics Enclosure)	Supported batteries: CR2032 or BR2032
CON9	RTC External Backup Power In 2[a]	Pin headers (2P) DF13-2P-1.25DS (20) (Hirose Electric)	Connector not mounted, supported batteries: CR2032 WK11 (Hitachi Maxell) or similar
CON10	RTC External Backup Power In 3[a]	Pin headers (2P) (2.54mm pitch)	Connector not mounted
SW1, SW2, SW3	User switch	Tact switch	
SW4, SW5, SW6	User switch	Tact switch	Switch not mounted
LED1	Power LED	LED (green, surface mount)	
LED2, LED3	User LED	LED (ϕ3mm)	LED not mounted

[a]CON8, CON9 and CON10 are external backup power in connectors for the RTC. It is possible to connect a separate external battery such as a lithium coin battery (CR or BR) in order to maintain time data during extended periods of no power supply. As all of the connectors are connected to the same terminals they cannot be used at the same time.

For the signals of each connector on the LCD Expansion Board, please refer to the "Armadillo-400 Series LCD Expansion Board Circuit Diagram" stored in the /document/hardware directory on the included DVD.

As CON2 and CON6 on the LCD Expansion Board are connected to the same signal lines they cannot be used at the same time. Please disconnect the Data Image LCD from CON2 when connecting another LCD module to CON6.

When connecting batteries aside from lithium coins (CR or BR) to the External RTC Backup Power In Connectors (CON9, CON10), please ensure that they do not exceed the rated maximum values of the equipped components as shown in the "Armadillo-400 Series LCD Expansion Board Circuit Diagram" stored in the /document/hardware directory on the included DVD.

9.1.3. Board Outline Diagrams

9.1.3.1. LCD Expansion Board (Product Revision A)

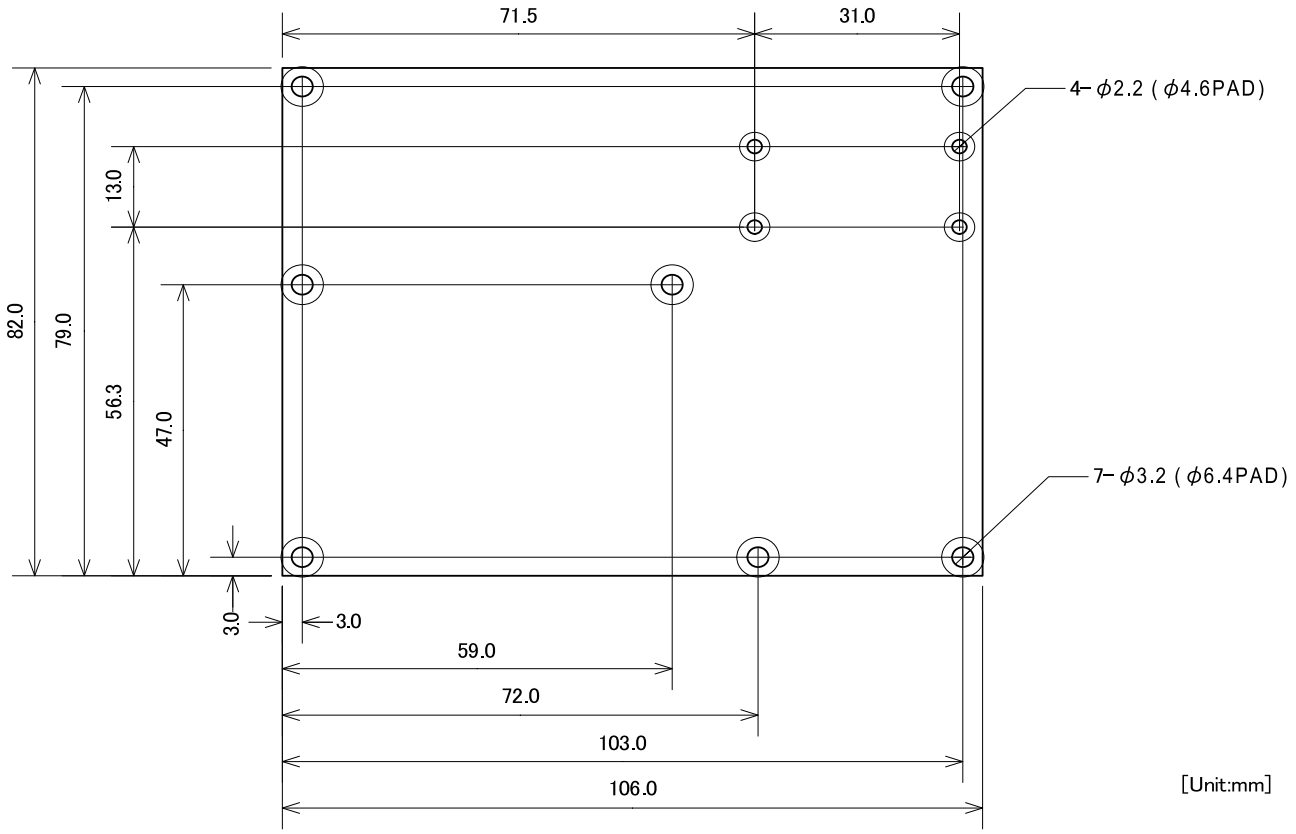


Figure 9.3. LCD Expansion Board (Product Revision A) Dimensions and Fixing Hole Measurements

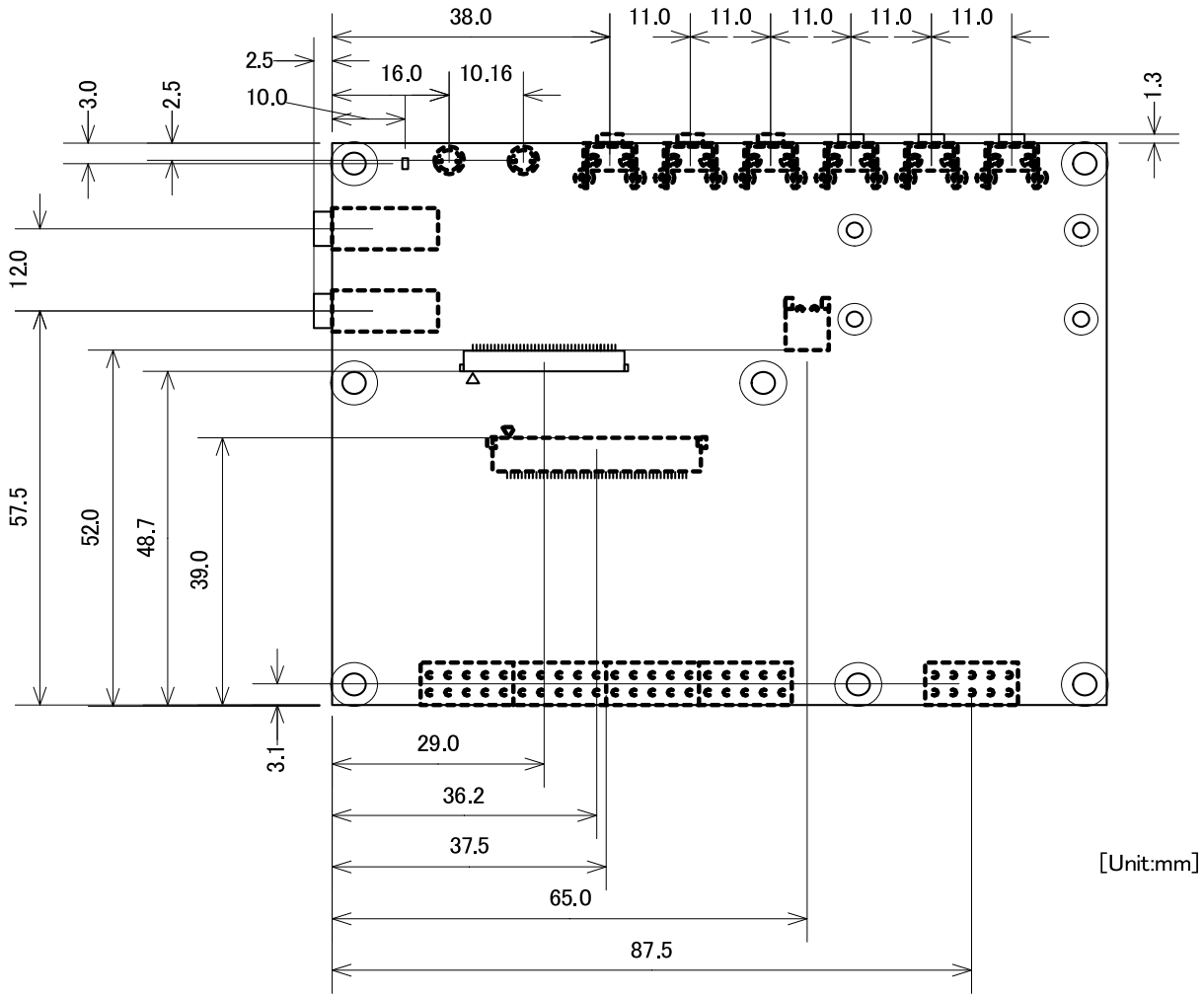


Figure 9.4. LCD Expansion Board (Product Revision A) Connector Locations

9.1.3.2. LCD Expansion Board (Product Revision B)

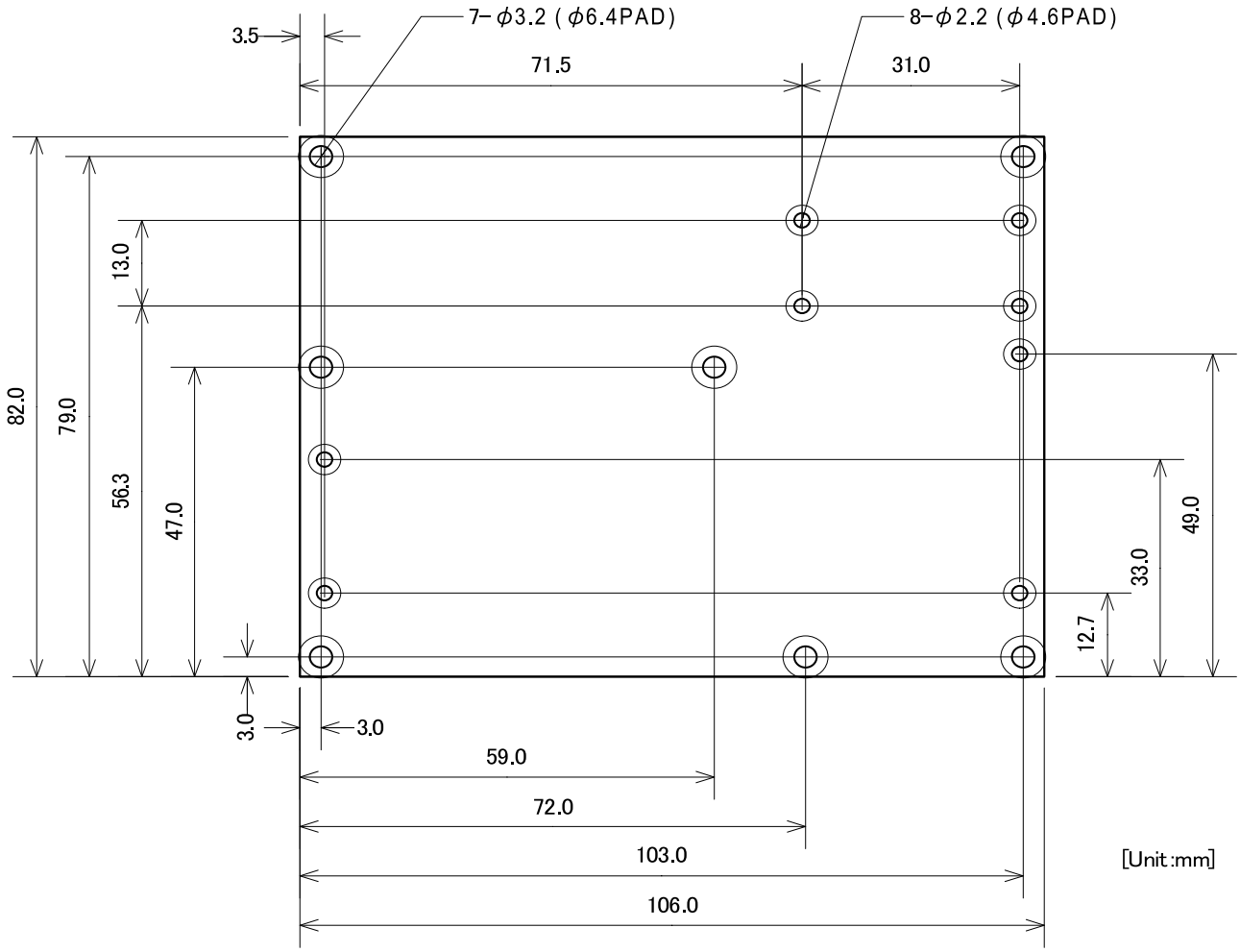


Figure 9.5. LCD Expansion Board (Product Revision B) Dimensions and Fixing Hole Measurements

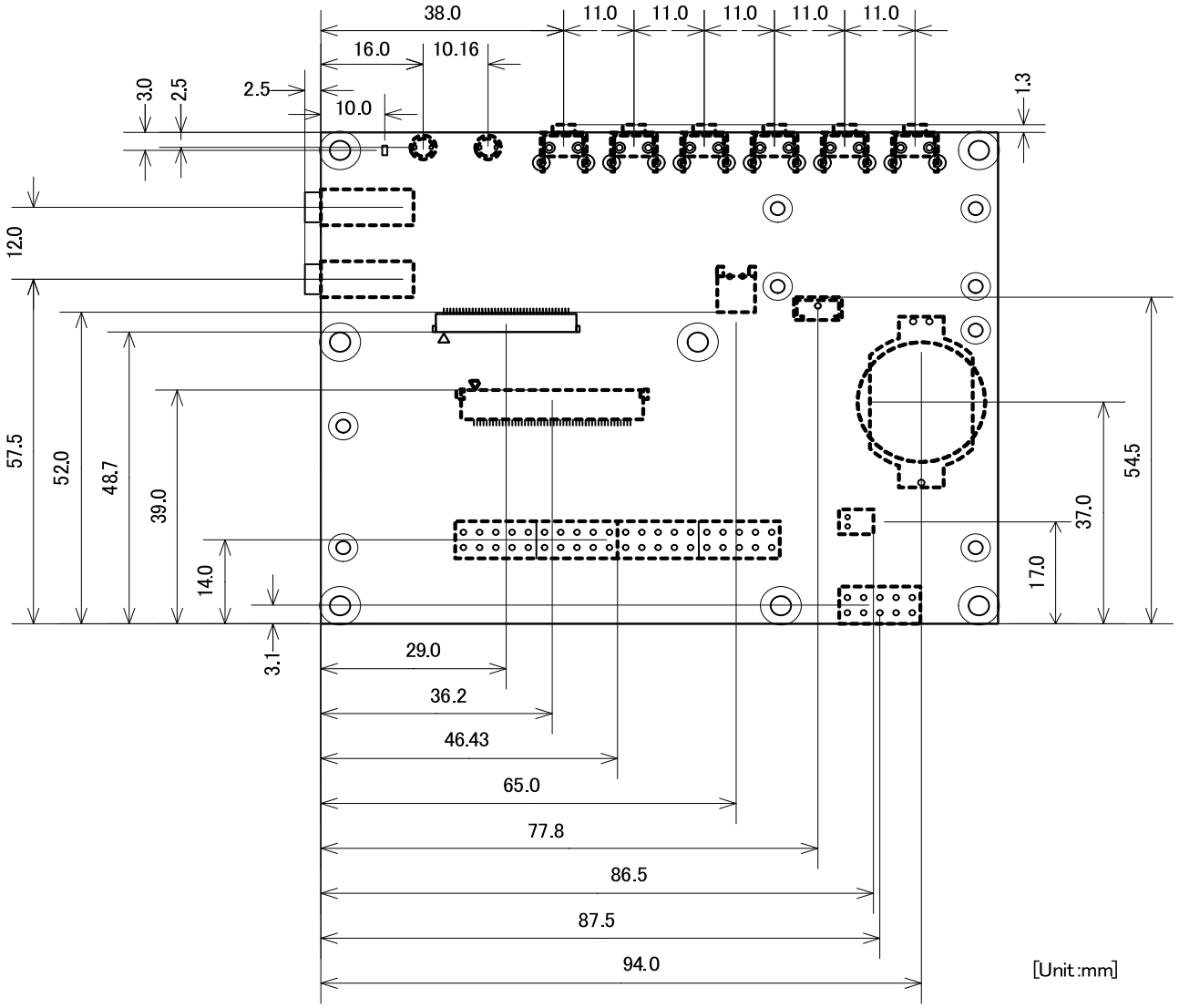


Figure 9.6. LCD Expansion Board (Product Revision B) Connector Locations

The LCD Expansion Board (Product Revision B) includes holes that can be used for metal fittings for fixing the LCD module in place. Reference dimensions and an assembly example of metal fittings using these holes are shown below.

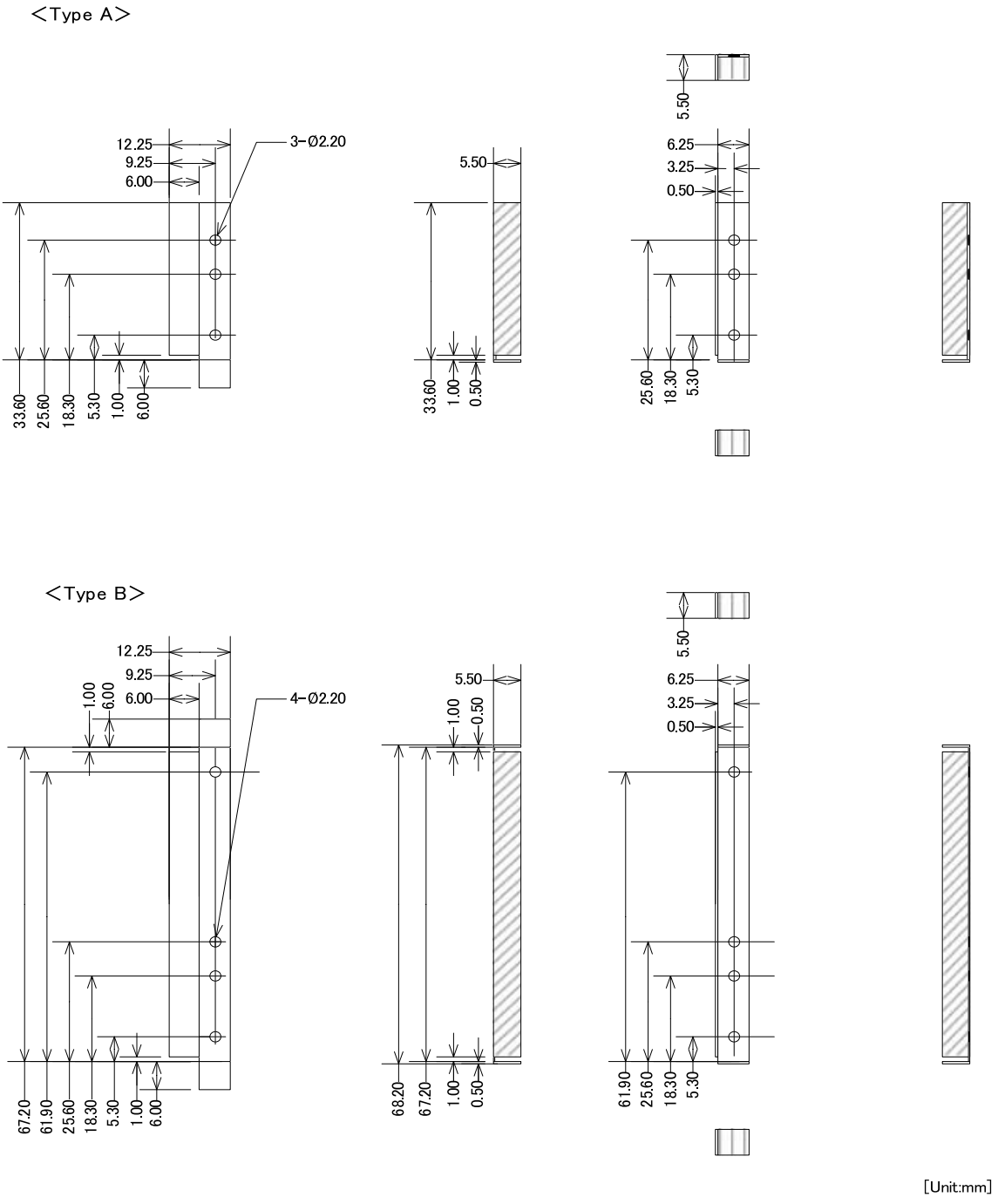


Figure 9.7. LCD Metal Fittings Reference Dimensions for LCD Expansion Board (Product Revision B)

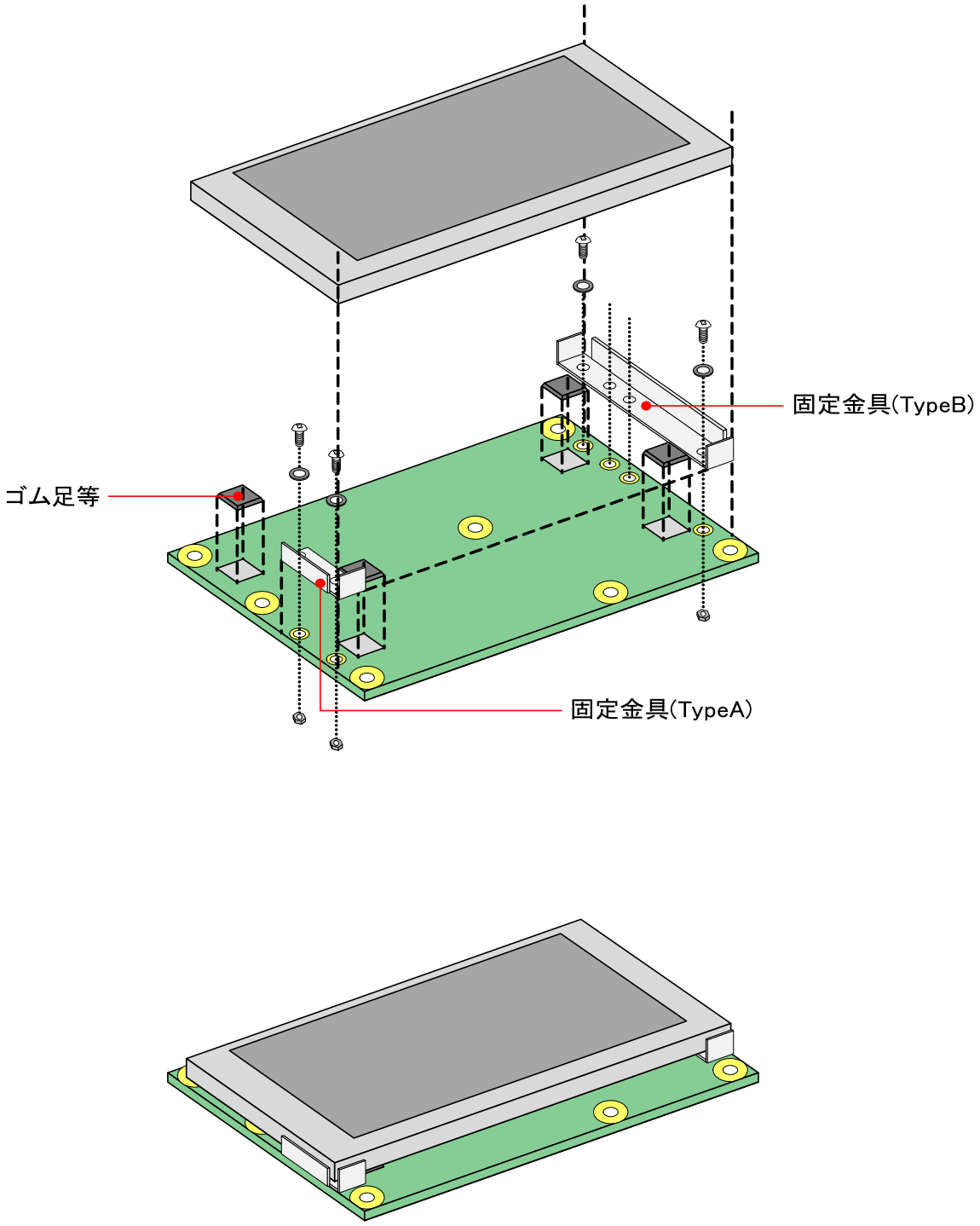


Figure 9.8. LCD Metal Fittings Assembly Example for LCD Expansion Board (Product Revision B)

9.1.4. Connections

The method of connecting the LCD and LCD Expansion board is shown in Figure 9.9, “LCD and LCD Expansion Board Connection”. To connect the LCD flexible board (FPC), after raising the lock lever of CON2 on the LCD Expansion Board push in the FPC until it stops and then lower the lock lever.

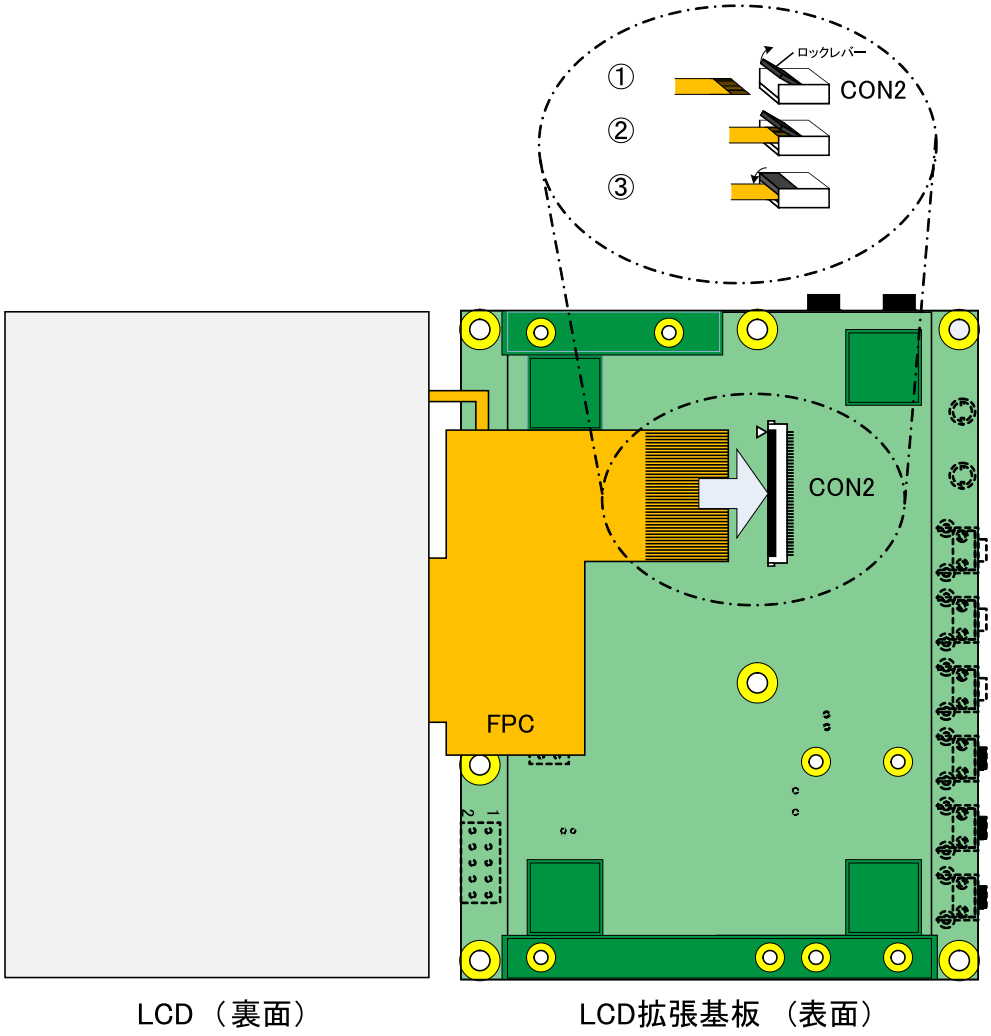


Figure 9.9. LCD and LCD Expansion Board Connection

Please take care when attaching the FPC as applying too much force to the lock lever of CON2 on the LCD Expansion Board may damage it.

The LCD is fixed to the LCD Expansion Board included in the Armadillo-440 LCD Model Development Set with double sided tape as shown in Figure 9.10, “LCD and LCD Expansion Board Fastening”.

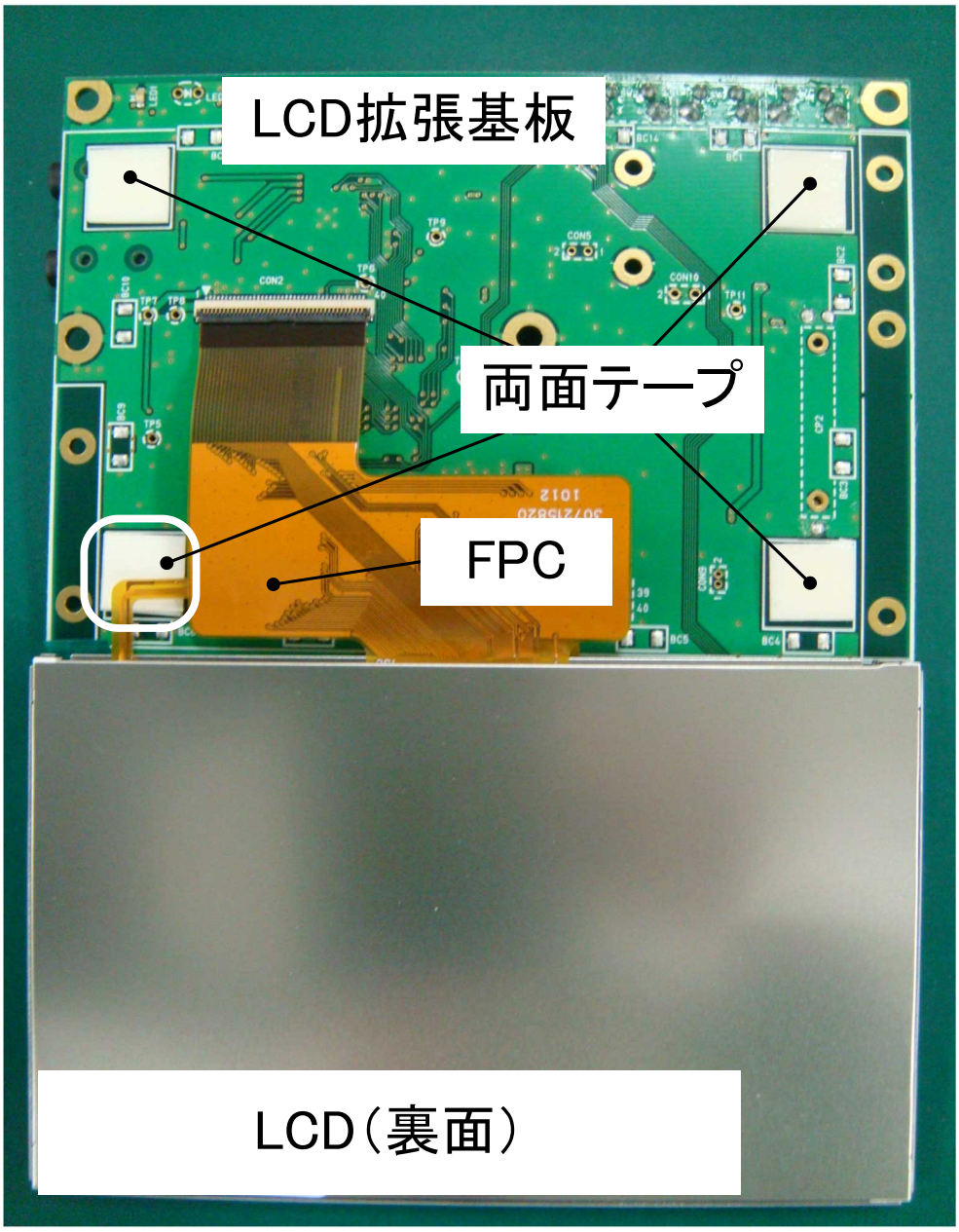


Figure 9.10. LCD and LCD Expansion Board Fastening

Please make sure that the LCD Expansion Board fitting is designed and used with safety in mind.

The use of double sided tape is not recommended for use in mass produced products for the following reasons. If using double sided tape, please keep safety in mind when doing so.

1) The adhesion of the double sided tape may deteriorate with aging and the LCD panel may fall off.

2) If the surface of the LCD panel is pressed strongly, the double sided tape may compact causing the LCD panel to touch and short with the LCD Expansion Board.

If using double sided tape, please pay full attention to the following points.

When affixing the included double sided tape to the specified places, it is placed so that it covers a part of the flexible print board (FPC). When pulling the LCD panel off the LCD Expansion Board, the FPC may be pulled still attached to the double sided tape causing it to snap.

Armadillo-440/460 and the LCD Expansion Board can be connected with a 0.5mm pitch 50 pin flexible flat cable (FFC). Connection examples are shown in Figure 9.12, “Connecting Armadillo-440 and LCD Expansion Board” and Figure 9.13, “Connecting Armadillo-460 and LCD Expansion Board”. To connect the FFC and the FFC connector, raise the lock lever on the FFC connector, push in the FFC until it stops and then lower the lock lever.

Please connect the FFC cable so that pin 1 of the FFC connector CON11 on Armadillo-440/460 is connected with pin 50 of the FFC connector CON1 on the LCD Expansion Board. As connecting pin 1 of CON1 and pin 1 of CON11 will mean that power and ground will short causing damage, please take full care when making the connection.

Please connect the FFC so that the electrodes are at the top side of the FFC connector CON11 on Armadillo-440/460 and the FFC connector CON1 on the LCD Expansion Board. If the FFC is connected so that the electrodes are on the under side, they may come in contact with the mounted components.

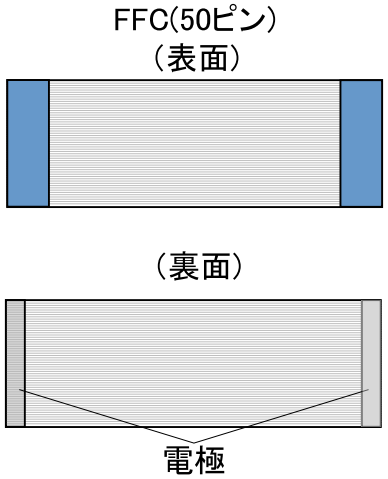


Figure 9.11. Flexible Flat Cable (FFC)

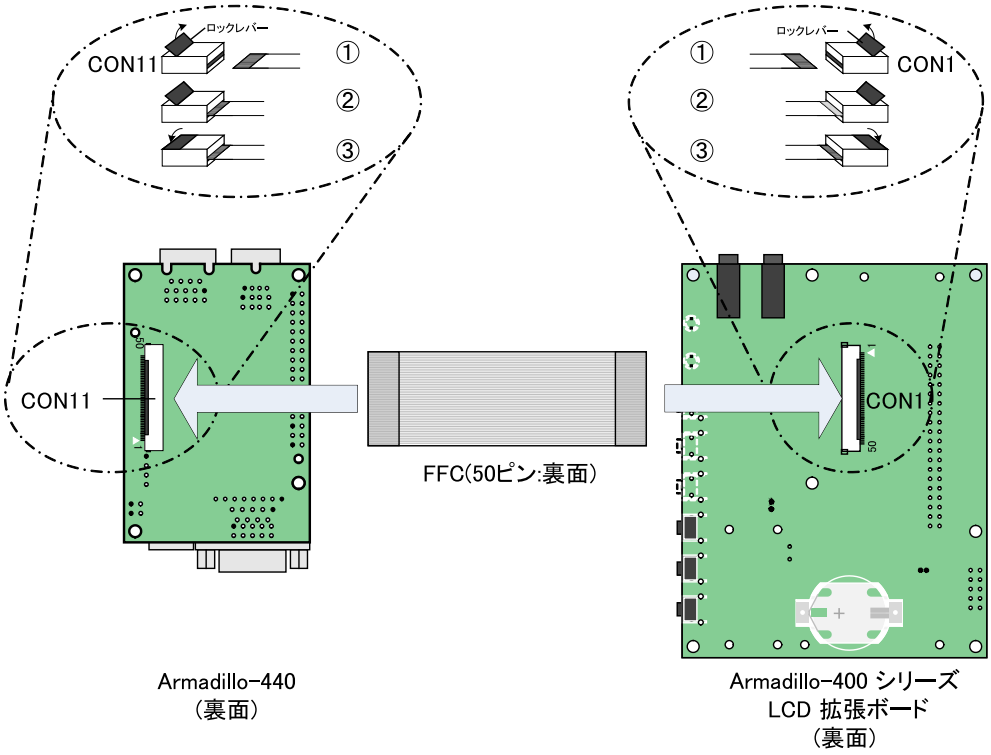


Figure 9.12. Connecting Armadillo-440 and LCD Expansion Board

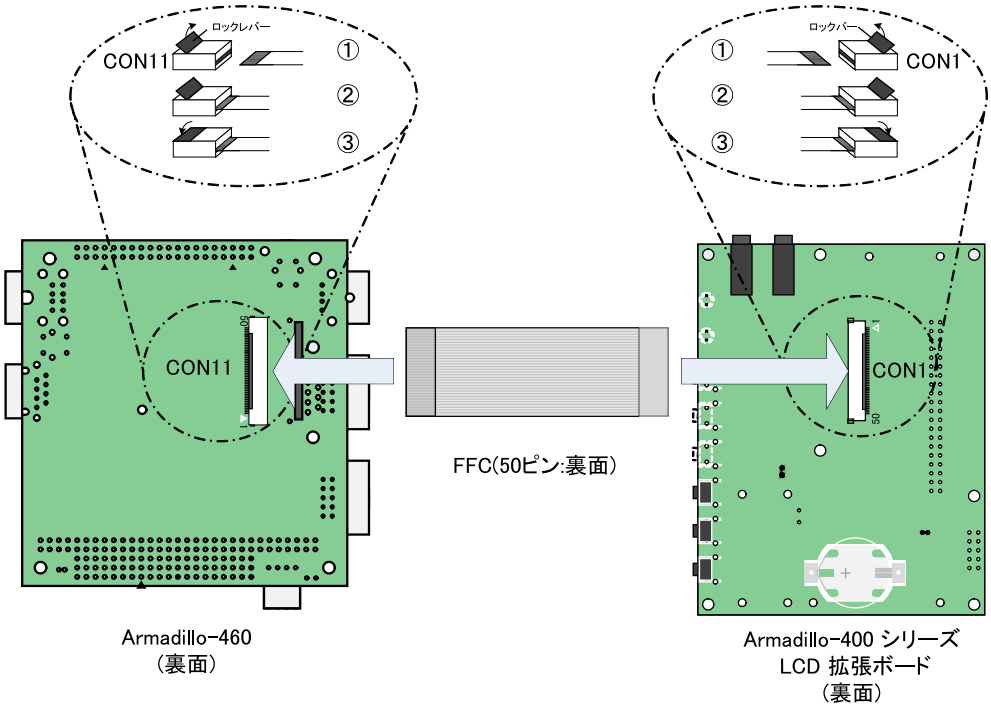


Figure 9.13. Connecting Armadillo-460 and LCD Expansion Board

The Armadillo-460 board has a slit which allows the FFC to be connected from either side of the board.

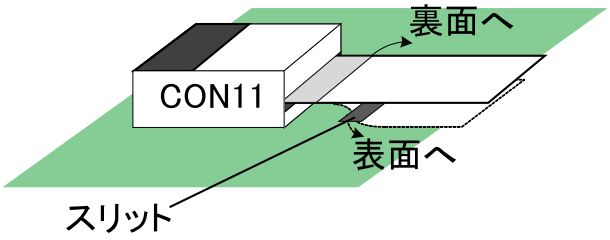


Figure 9.14. Armadillo-460 Slit

9.1.5. About Defective LCD Pixels

Defective pixels occur at a certain rate due to the fundamental properties of LCD panels. The tolerance range of defective pixels in panels used on the LCD Expansion Board follow the standards set out below.

9.1.5.1. Pixel Defect Definitions

Table 9.5. Pixel Defect Definitions

Bright Dots	Pixels which appear brighter than surrounding pixels of the same color on an all-black screen display.
Dark Dots	Pixels which appear darker than surrounding pixels of the same color on an all-white screen display.
Continuous Dot Defects	Where multiple bright or dark dot defects occur continuously. This applies to both bright-bright and dark-dark dot defects.

9.1.5.2. Examination Standard

Table 9.6. Defect Tolerance Range

Defect	Tolerance Range
Bright Dot Defects	4
Dark Dot Defects	5
2 Dot Continuous Defects	2 groups (bright dots) 3 groups (dark dots)
3 Or More Dot Continuous Defects	0 (bright or dark dots)
Total Defects	5

9.2. Armadillo-400 Series RTC Option Module (Product ID: OP-A400RTCMOD-00)

9.2.1. Board Overview

The Armadillo-400 Series RTC Option Module (hereafter RTC Option Module) is a board that connects to Expansion Interface 2 (CON14). The board incorporates a Seiko Instruments Inc. real-time clock (hereafter RTC). An electric double-layer capacitor provides backup power to the RTC allowing it to function for a period of time even after power to the board has been cut. It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

The CON14 signal can be used for transmission when it is set to I2C2 in i.MX257's multiplex function.

The main specifications of the RTC Option Module are as follows.

Table 9.7. RTC Option Module (Product ID: OP-A400RTCMOD-00) Specifications

Real-Time Clock (RTC)	Seiko Instruments RTC (S-35390A)
Backup	Approximately 5 days (environmental temperature of 25℃, reference value) external battery can be connected to External RTC Backup Connector (CON2)
Board Size	10.0 x 22.0 mm
Power Supply Voltage	DC2.0 - 3.3V
Operating Temperature	-10 - 60℃ (with no condensation)

The time accuracy of the RTC is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

As the backup time of the RTC is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

The RTC backup electric double-layer capacitor (Panasonic EECEN0F204RK) equipped on the RTC Option Module (Product ID: OP-A400RTCMOD-00) has a finite lifetime. Its capacity diminishes over time while its internal resistance increases.

The "10℃ Double Rule" can generally be applied for the lifetime estimate of electric double-layer capacitors.

$$Lx = Lo \times 2^{((To-Tx)/10)}$$

Here, Lo is guaranteed lifetime (hours) at the maximum temperature, Lx is estimated lifetime (hours) of actual use, To is the maximum temperature (℃), and Tx is the actual use environmental temperature (℃).

The guaranteed durability values published by the maker for EECEN0F204RK are 500 hours at +60℃ (capacitance change within ±30% of original, internal resistance less than 4kΩ). Supposing the environmental temperature was 25℃, the estimated lifetime would be as follows.

$$Tx = 500 \times 2^{((60-25)/10)} = 5600 \text{ hours approx.}$$

Note that as the lifetime of electric double-layer capacitors is effected by the length of time voltage is applied and not the number of charge cycles, the time calculated above is the cumulative operating time.

If the prescribed lifetime is exceeded, abrupt characteristic degradation and liquid leaking may occur. If using in mass produced products where long term continuous operation is expected, please carry out regular inspections and replacements.

9.2.2. Interface Layout

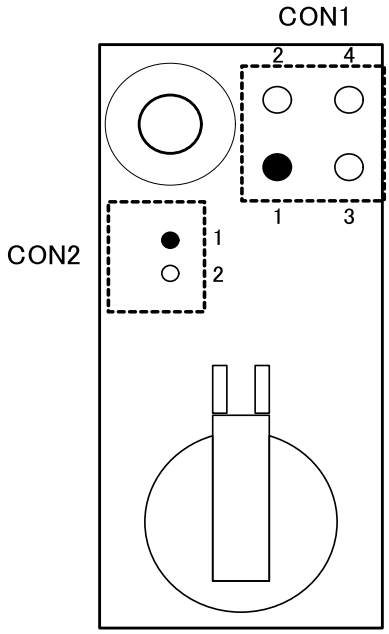


Figure 9.15. RTC Option Module (Product ID: OP-A400RTCMOD-00) Interface Layout

Table 9.8. RTC Option Module (Product ID: OP-A400RTCMOD-00) Interface Details

Part Number	Interface	Shape	Notes
CON1	Armadillo-400 Series connection	Pin socket (4P) (2.54mm pitch)	
CON2	RTC external backup power in[a]	Pin headers (2P) DF13-2P-1.25DSA (Hirose Electric)	Supported battery: CR2032 WK11 (Hitachi Maxell or similar)

[a]For the circuit layout of the External RTC Backup Power In Connector (CON2), please refer to the "Armadillo-400 Series RTC Option Module Circuit Diagram" stored in the /document/hardware directory on the included DVD.

When connecting batteries aside from lithium coins (CR or BR) to the External RTC Backup Power In Connector (CON2), please ensure that they do not exceed the rated maximum values of the equipped components as shown in the "Armadillo-400 Series RTC Option Module Circuit Diagram" stored in the /document/hardware directory on the included DVD.

9.2.3. Board Outline Diagrams

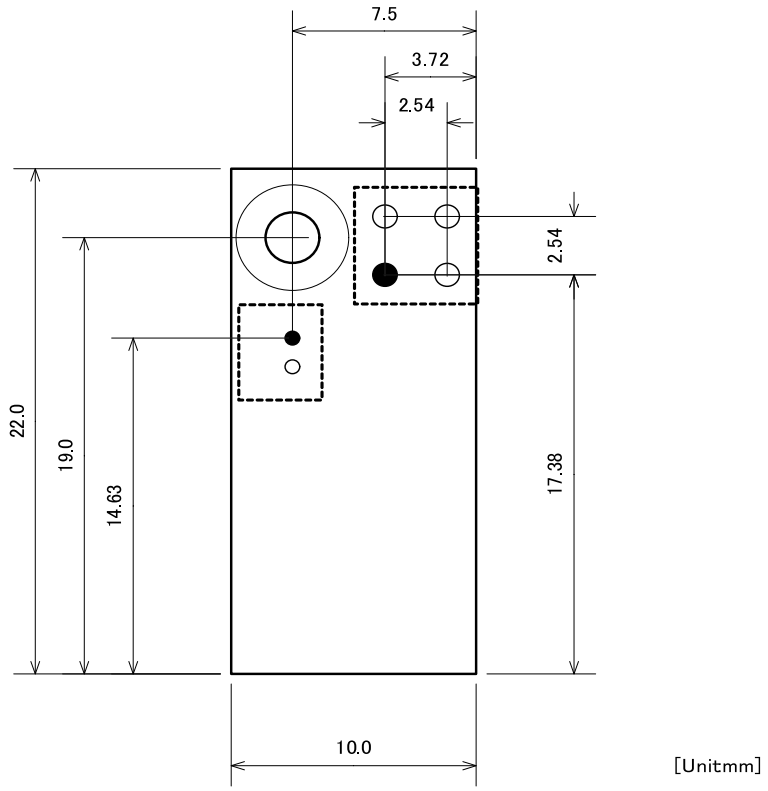


Figure 9.16. RTC Option Module (Product ID: OP-A400RTCMOD-00) Dimensions

9.2.4. Assembly

While the following describes assembly with Armadillo-420/440, the same method can be used with Armadillo-460.

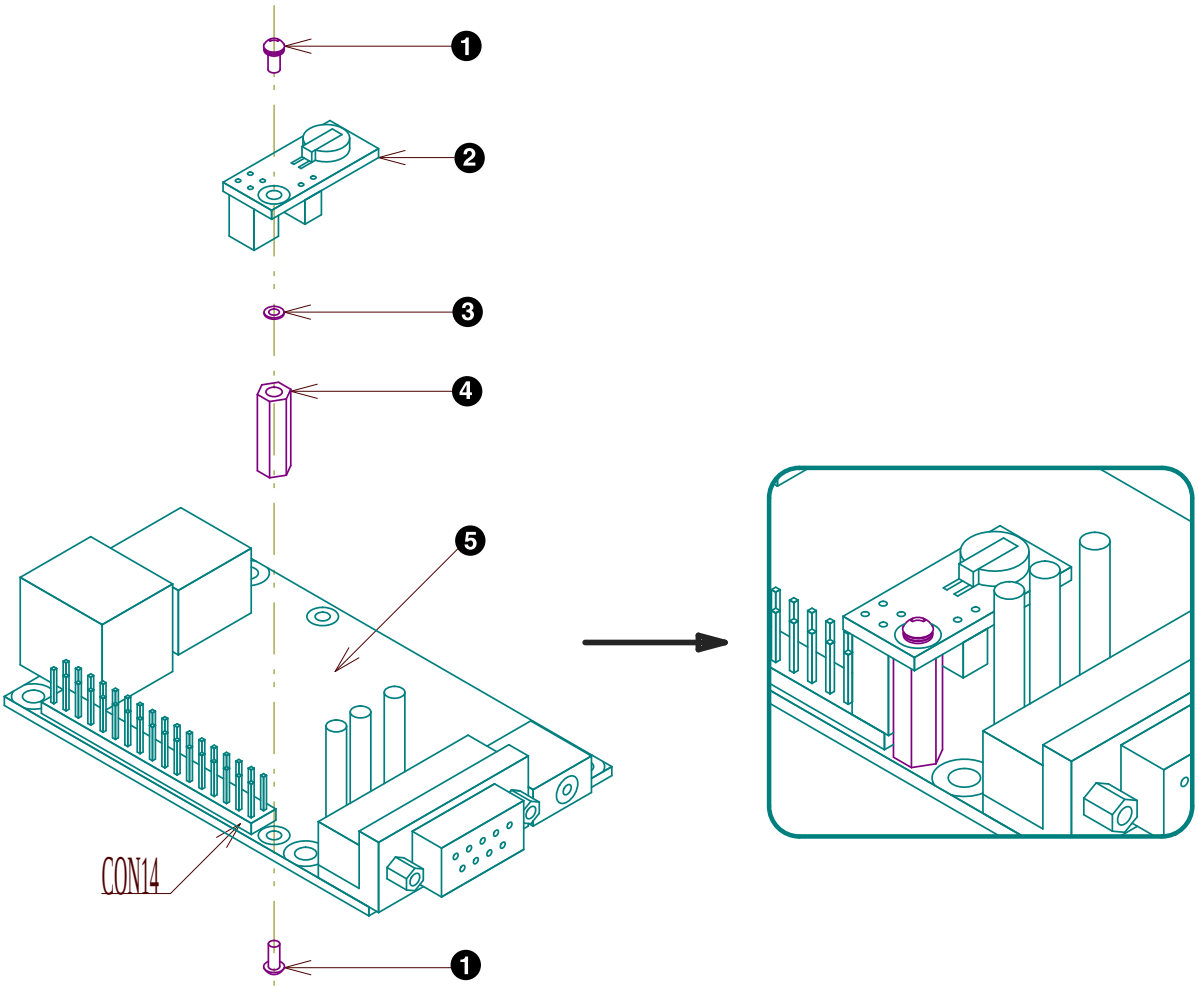


Figure 9.17. RTC Option Module (Product ID: OP-A400RTCMOD-00) Assembly Diagram

1. Round head screw (M2, L=6mm, spring washer + small washer)
2. RTC Option Module
3. Flat washer
4. Metal spacer (M2, L=11mm, D=4mm)
5. Armadillo-400 Series

9.3. Armadillo-400 Series RTC Option Module (Product ID: OP-A400RTCMOD-01)

9.3.1. Board Overview

The Armadillo-400 Series RTC Option Module (hereafter RTC Option Module) is a board that connects to Expansion Interface 2 (CON14). The board incorporates a Seiko Instruments Inc. real-time clock (hereafter RTC). A laminated ceramic capacitor provides backup power to the RTC allowing it to function for a few minutes even after power to the board has been cut. It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

The CON14 signal can be used for transmission when it is set to I2C2 in i.MX257's multiplex function.

The main specifications of the RTC Option Module are as follows.

Table 9.9. RTC Option Module (Product ID: OP-A400RTCMOD-01) Specifications

Real-Time Clock (RTC)	Seiko Instruments RTC (S-35390A)
Backup	300sec (typ.), 60sec (min.) external battery can be connected to External RTC Backup Connector (CON2)
Board Size	10.0 x 22.0 mm
Power Supply Voltage	DC2.0 - 3.5V
Operating Temperature	-20 - 70℃ (with no condensation)

The time accuracy of the RTC is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

As the backup time of the RTC is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

9.3.2. Interface Layout

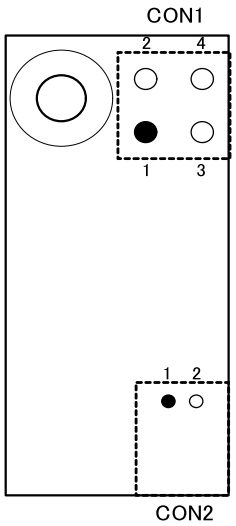


Figure 9.18. RTC Option Module (Product ID: OP-A400RTCMOD-01) Interface Layout

Table 9.10. RTC Option Module (Product ID: OP-A400RTCMOD-01) Interface Details

Part Number	Interface	Shape	Notes
CON1	Armadillo-400 Series connection	Pin socket (4P) (2.54mm pitch)	
CON2	RTC external backup power in[a]	Pin headers (2P) DF13-2P-1.25DSA (Hirose Electric)	Supported battery: CR2032 WK11 (Hitachi Maxell or similar)

[a]For the circuit layout of the External RTC Backup Power In Connector (CON2), please refer to the "Armadillo-400 Series RTC Option Module Circuit Diagram" stored in the /document/hardware directory on the included DVD.

When connecting batteries aside from lithium coins (CR or BR) to the External RTC Backup Power In Connector (CON2), please ensure that they do not exceed the rated maximum values of the equipped components as shown in the "Armadillo-400 Series RTC Option Module Circuit Diagram" stored in the /document/hardware directory on the included DVD.

9.3.3. Board Outline Diagrams

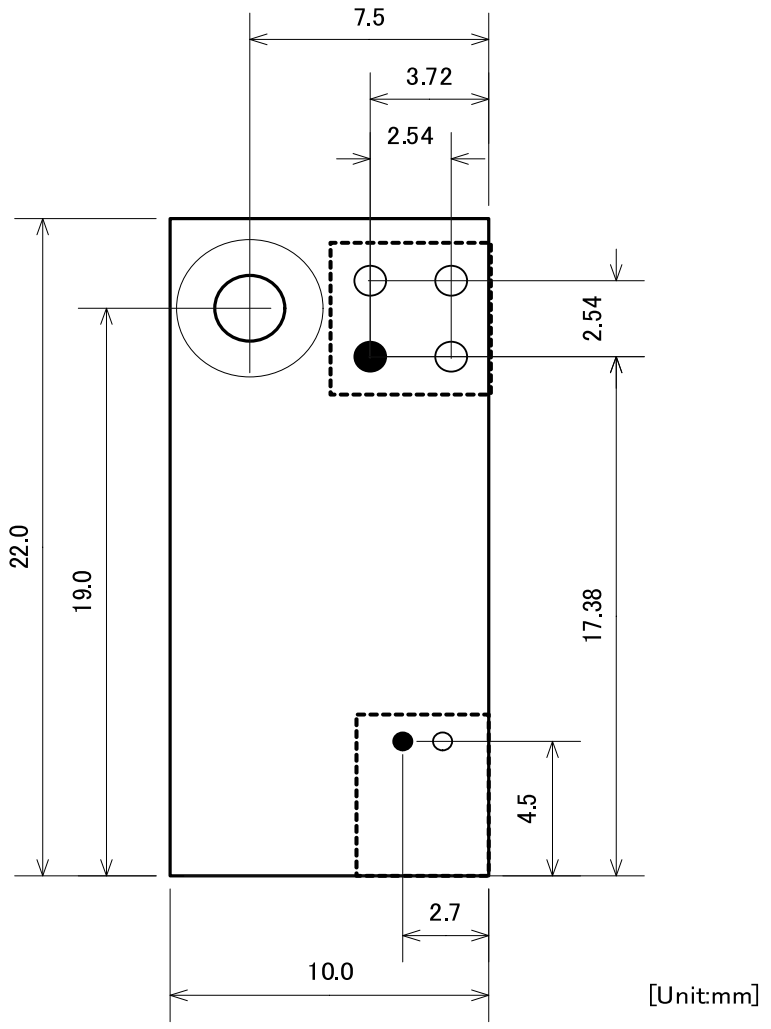


Figure 9.19. RTC Option Module (Product ID: OP-A400RTCMOD-01) Dimensions

9.3.4. Assembly

While the following describes assembly with Armadillo-420/440, the same method can be used with Armadillo-460.

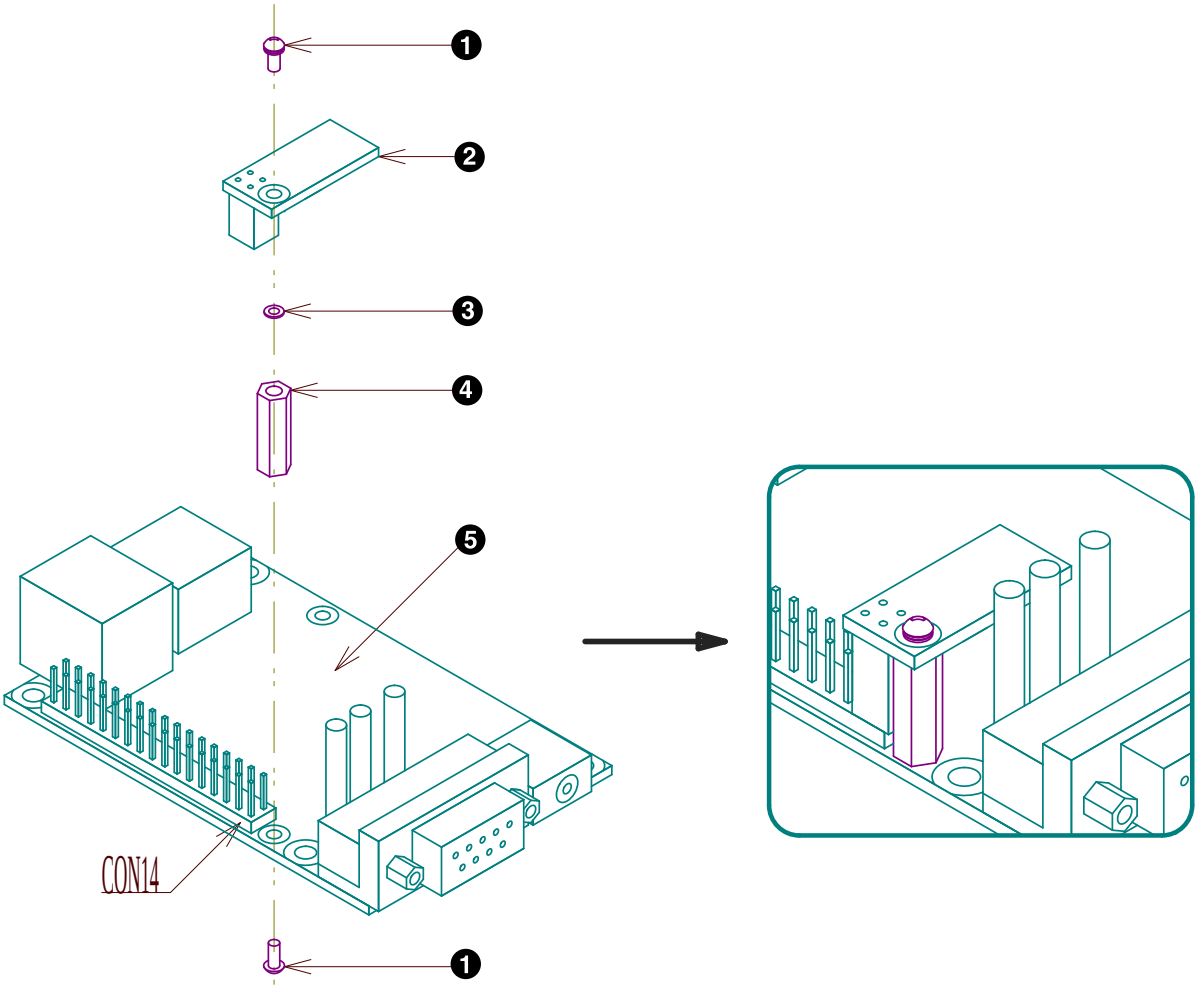


Figure 9.20. RTC Option Module (Product ID: OP-A400RTCMOD-01) Assembly Diagram

1. Round head screw (M2, L=6mm, spring washer + small washer)
2. RTC Option Module
3. Flat washer
4. Metal spacer (M2, L=11mm, D=4mm)
5. Armadillo-400 Series

9.4. Armadillo-400 Series WLAN Option Module (AWL12 Compatible) (Product ID: OP-A400-AWLMOD-00)

9.4.1. Board Overview

The Armadillo-400 Series WLAN Option Module (AWL12 Compatible) (hereafter WLAN Option Module (AWL12 Compatible)) is a board that connects to the expansion interfaces (CON9, CON14) on the Armadillo-400 Series. It is comprised of the Armadillo-WLAN module (hereafter AWL12) and the Armadillo-400 Series WLAN Interface Board (AWL12 Compatible) (hereafter WLAN Interface Board (AWL12 Compatible)). The WLAN Option Module (AWL12 Compatible) incorporates a Seiko Instruments Inc. real-time clock (hereafter RTC). A laminated ceramic capacitor provides backup power to the RTC allowing it to function for a few minutes even after power to the board has been cut. It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

The CON9 and CON14 signals can be used for transmission when set to SDHC2 or I2C2 in i.MX257's multiplex function.

The main specifications of the WLAN Option Module (AWL12 Compatible) are as shown below. For more detailed specifications on the AWL12, please refer to the Armadillo-WLAN (AWL12) Hardware Manual on the Armadillo Site product manual page.

Table 9.11. WLAN Option Module (AWL12 Compatible) Specifications

Wireless LAN Module	Armadillo-WLAN Module (AWL12-U00Z) equipped
Real-Time Clock (RTC)	Seiko Instruments RTC (S-35390A)
Backup	300sec (typ.), 60sec (min.) External battery can be connected via RTC External Backup Connectors (CON5、CON6、CON7)
Board Size	41.0 x 50.0 mm
Power Supply Voltage	DC3.3±0.2V
Operating Temperature	-20 - 70℃ (with no condensation)

The time accuracy is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

As the backup time of the RTC is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

The Armadillo-400 Series WLAN Interface Board (AWL12 Compatible) Circuit Diagram is stored in the /document/hardware directory on the included DVD.

9.4.2. Interface Layout

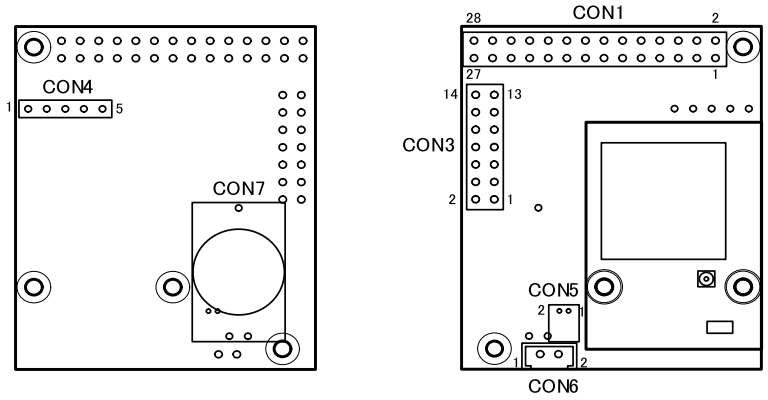


Figure 9.21. WLAN Option Module (AWL12 Compatible) Interface Layout

Table 9.12. WLAN Option Module (AWL12 Compatible) Interface Details

Symbol	Interface	Shape	Notes
CON1	Armadillo-400 Series connection	Pin socket (28P) (2.54mm pitch)	
CON3	SPI	Pin headers (14P) (2.54mm pitch)	Connector not mounted
CON4	Serial	Pin headers (5P) (2.54mm pitch)	Connector not mounted
CON5	RTC external backup power in 1	Pin headers (2P) (1.25mm pitch) DF13-2P-1.25DS (20) (Hirose Electric)	Supported battery: CR2032 WK11 (Hitachi Maxell or similar)
CON6	RTC external backup power in 2	Pin headers (2P) (2.54mm pitch)	Connector not mounted
CON7	RTC external backup power in 3	Battery holder HU1220 (Takachi Electronics Enclosure)	Connector not mounted Supported batteries: CR1220 or BR1220

9.4.2.1. CON1 Armadillo-400 Series Connection Connector

This connector is for connecting to the Armadillo-400 Series Expansion Interface (CON9, CON14).

Table 9.13. WLAN Option Module (AWL12 Compatible) CON1 Signals

Pin Number	Signal Name	I/O	Function
1	+3.3V_IO	Power	Power (+3.3V_IO)
2	GND	Power	Power (GND)
3	I2C2_SCL	In	RTC I2C Clock
4	I2C2_SDA	In/Out	RTC I2C Data
5	SD_PWREN*	In	SD Power Enable Signal (0:ON, 1:OFF)
6	RTC_INT1*	Out	RTC Interrupt Signal
7	NC	-	-

Pin Number	Signal Name	I/O	Function
8	UART5_RXD	Out	UART Data Receive Connected to CON4 (pin 2) on WLAN Option Module (AWL12 Compatible)
9	NC	-	-
10	UART5_TXD	In	UART Data Send Connected to CON4 (pin 3) on WLAN Option Module (AWL12 Compatible)
11	+3.3V_IO	Power	Power (+3.3V_IO)
12	+3.3V_IO	Power	Power (+3.3V_IO)
13	GND	Power	GND
14	GND	Power	GND
15	NC	-	-
16	NC	-	-
17	NC	-	-
18	NC	-	-
19	SD2_WP	-	Pull-down (10kΩ resistance)
20	SD2_CMD	In/Out	Connected to SDCMD signal line on AWL12
21	SD2_CD*	-	Pull-down (10kΩ resistance)
22	SD2_CLK	In	Connected to SDCLK signal line on AWL12
23	GND	Power	GND
24	+3.3V_IO	Power	Power (+3.3V_IO)
25	SD2_DAT0	In/Out	Connected to SDDATA0 signal line on AWL12
26	SD2_DAT1	In/Out	Connected to SDDATA1 signal line on AWL12
27	SD2_DAT2	In/Out	Connected to SDDATA2 signal line on AWL12
28	SD2_DAT3	In/Out	Connected to SDDATA3 signal line on AWL12

9.4.2.2. CON3 SPI Interface

This is a connector for the SPI interface signals on the AWL12.

Table 9.14. WLAN Option Module (AWL12 Compatible) CON3 Signals

Pin Number	Signal Name	I/O	Function
1	+3.3V_IO	Power	Power (+3.3V_IO)
2	GND	Power	GND
3	RST	In	Connected to RST signal line on AWL12
4	SPI_RDY	Out	Connected to SPI_RDY signal line on AWL12
5	HOSTINT	Out	Connected to HOSTINT signal line on AWL12
6	WAKEUP	In	Connected to WAKEUP signal line on AWL12
7	SPI_FS	In	Connected to SPI_FS signal line on AWL12
8	SPI_RXD	In	Connected to SPI_RXD signal line on AWL12
9	SPI_TXD	Out	Connected to SPI_TXD signal line on AWL12
10	SPI_CLK	In	Connected to SPI_CLK signal line on AWL12
11	NC	-	-
12	NC	-	-
13	BOOT3	In	Connected to BOOT3 signal line on AWL12
14	GND	Power	GND

9.4.2.3. CON4 Serial interface

Table 9.15. WLAN Option Module (AWL12 Compatible) CON4 Signals

Pin Number	Signal Name	I/O	Function
1	NC		
2	UART5_RXD	In	Connected to CON1 (pin 8) on WLAN Option Module (AWL12 Compatible)
3	UART5_TXD	Out	Connected to CON1 (pin 10) on WLAN Option Module (AWL12 Compatible)
4	+3.3V_IO	Power	Power (+3.3V_IO)

Pin Number	Signal Name	I/O	Function
5	GND	Power	GND

9.4.2.4. CON5, CON6, CON7 External RTC Backup Connectors

These are external backup connectors for the RTC equipped on the WLAN Option Module (AWL12 Compatible). It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

Table 9.16. WLAN Option Module (AWL12 Compatible) CON5, CON6 Signals

Pin Number	Signal Name	I/O	Function
1	BAT	Power	RTC external backup power in
2	GND	Power	GND

As CON5, CON6 and CON7 are connected to the same terminals they cannot be used at the same time.

When connecting batteries aside from lithium coins (CR or BR) to the External RTC Backup Connectors (CON5, CON6), please ensure that they do not exceed the rated maximum values of the equipped components as shown in the "Armadillo-400 Series WLAN Interface Board (AWL12 Compatible) Circuit Diagram" stored in the /document/hardware directory on the included DVD.

9.4.3. Board Outline Diagrams

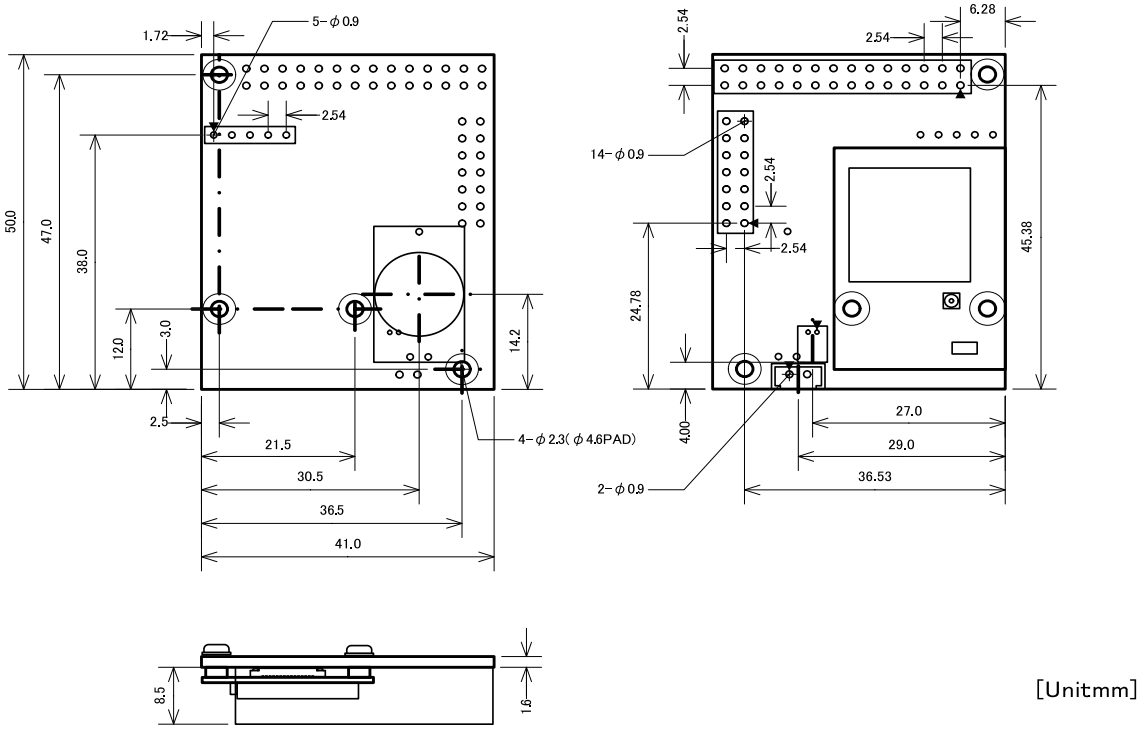


Figure 9.22. WLAN Option Module (AWL12 Compatible) Dimensions

9.4.4. Assembly

While the following describes assembly with Armadillo-420/440, the same method can be used with Armadillo-460.

9.4.4.1. AWL12 And WLAN Interface Board (AWL12 Compatible) Assembly

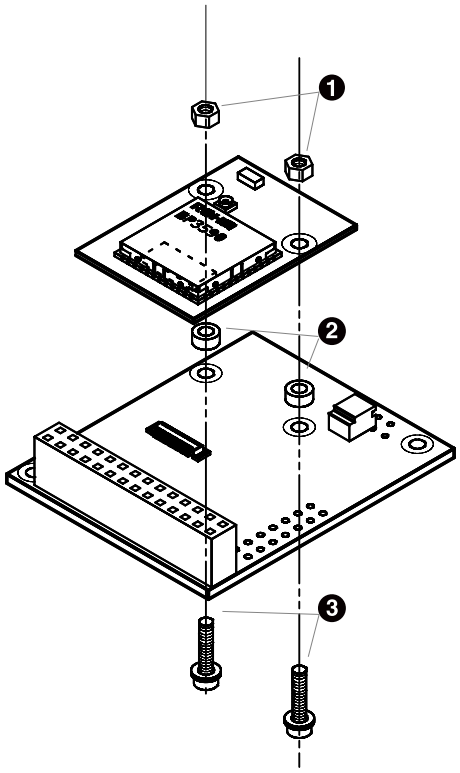


Figure 9.23. AWL12 and WLAN Interface Board (AWL12 Compatible) Assembly Diagram

1. Nut (M2, L=1.6mm, D=4mm)
2. Metal spacer (M2, L=1.5mm, D=4mm)
3. Round head screw (M2, L=8mm, spring washer + small washer)

Position the connectors on the AWL12 and WLAN Interface Board (AWL12 Compatible) together and then connect them. Please take care as applying too much force may cause damage.

9.4.4.2. WLAN Option Module (AWL12 Compatible) and Armadillo-400 Series Assembly

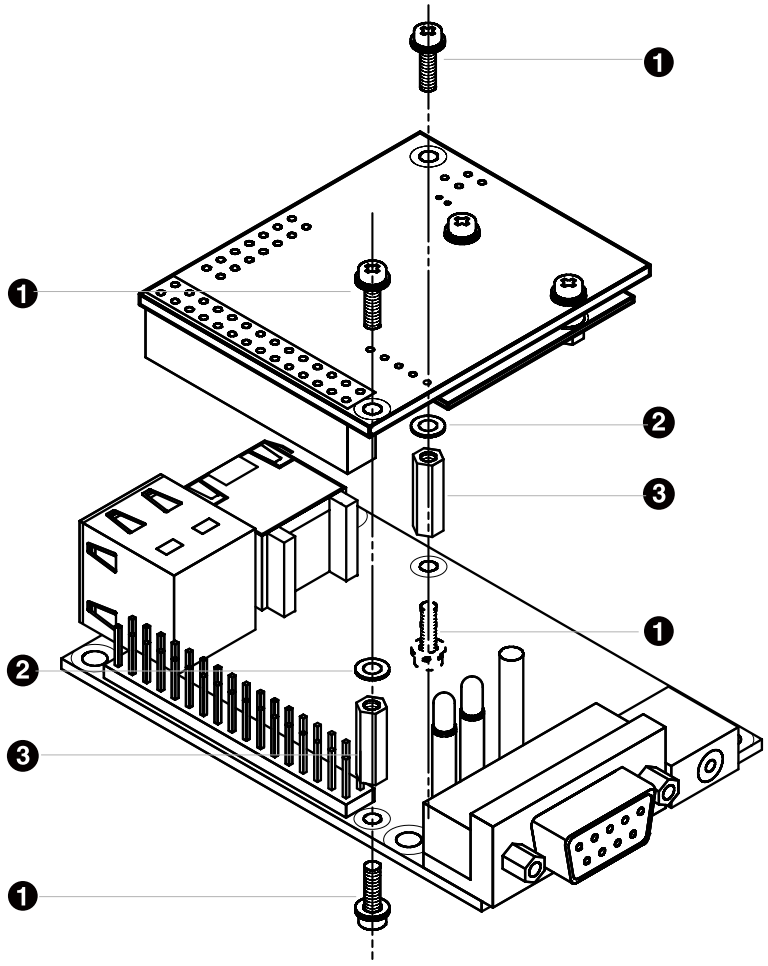


Figure 9.24. WLAN Option Module (AWL12 Compatible) and Armadillo-400 Series Assembly Diagram

1. Round head screw (M2, L=6mm, spring washer + small washer)
2. Metal spacer (M2, L=11mm, D=4mm)
3. Washer (M2, L=0.3mm, D=4.3mm)

9.4.4.3. WLAN Option Module (AWL12 Compatible) And External Antenna Assembly (For Evaluation and Development)

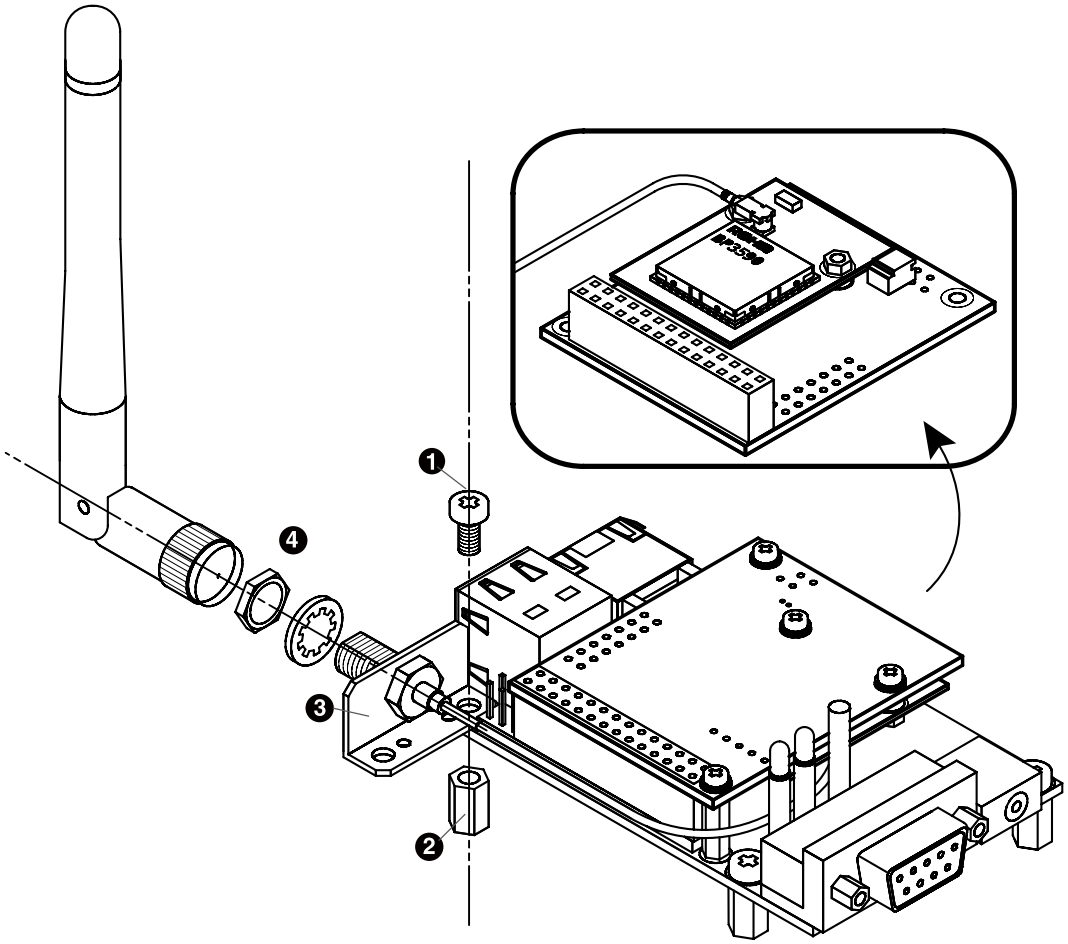


Figure 9.25. WLAN Option Module (AWL12 Compatible) and External Antenna Assembly Diagram (For Evaluation and Development)

1. Round head screw (M3, L=5mm)
2. Plastic spacer (M3, L=8mm, D=5.5mm)
3. External Antenna Metal Fitting
4. External Antenna

When connecting the external antenna cable to the antenna terminal on the AWL12, please be careful not to apply too much force as it may cause damage.

When removing the external antenna cable, it is recommended to use a dedicated removal tool (U.FL-LP-N-2 Hirose Electric). Doing so without a dedicated removal tool may cause the connector to deform or the cable to break.

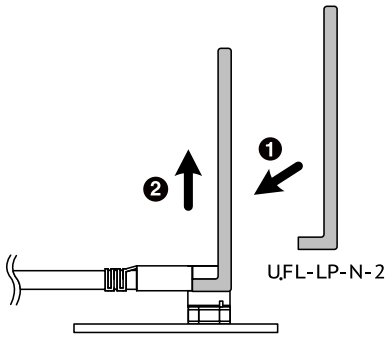


Figure 9.26. External Antenna Cable Removal

If an external antenna cable is connected to the antenna terminal on the AWL12 for an extended period of time, the switch in the coaxial connector may not return. If it does not return, the chip antenna will no longer be usable.

During evaluation and development, when not using the WLAN Option Module (AWL12 Compatible) for a long period of time please store it after having removed the external antenna cable from the antenna terminal on the AWL12. Also, when employing the WLAN Option Module (AWL12 Compatible) as part of a mass produced product, it is not recommended to switch from the external antenna to the chip antenna connection.

9.5. Armadillo-400 Series WLAN Option Module (AWL13 Compatible) (Product ID: OP-A400-AWLMOD-10)

9.5.1. Board Overview

The Armadillo-400 Series WLAN Option Module (AWL13 Compatible) (hereafter WLAN Option Module (AWL13 Compatible)) is a board that connects to the expansion interfaces (CON9, CON14) on the Armadillo-400 Series. It is comprised of the Armadillo-WLAN module (hereafter AWL13) and the Armadillo-400 Series WLAN Interface Board (AWL13 Compatible) (hereafter WLAN Interface Board (AWL13 Compatible)). The WLAN Option Module (AWL13 Compatible) incorporates a Seiko Instruments Inc. real-time clock (hereafter RTC). A laminated ceramic capacitor provides backup power to the RTC allowing it to function for a few minutes even after power to the board has been cut. It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

The CON9 and CON14 signals can be used for transmission when set to SDHC2 or I2C2 in i.MX257's multiplex function.

The main specifications of the WLAN Option Module (AWL13 Compatible) are as shown below. For more detailed specifications on the AWL13, please refer to the Armadillo-WLAN (AWL13) Hardware Manual on the Armadillo Site product manual page.

Table 9.17. WLAN Option Module (AWL13 Compatible) Specifications

Wireless LAN Module	Armadillo-WLAN Module (AWL13-U00Z) equipped
Real-Time Clock (RTC)	Seiko Instruments RTC (S-35390A)
Backup	300sec (typ.), 60sec (min.) External battery can be connected via RTC External Backup Connectors (CON5、CON6、CON7)
Board Size	41.0 x 50.0 mm
Power Supply Voltage	DC3.3±0.2V
Operating Temperature	-20 - 70℃ (with no condensation)

The time accuracy is approximately ±30 seconds per month average at an environment temperature of 25℃ (reference value only). As the accuracy is highly dependent on environmental temperature, please make sure to check all relevant characteristics before use.

As the backup time of the RTC is highly dependent on environmental temperature and length of voltage supply etc, please make sure to check all relevant characteristics before use.

The Armadillo-400 Series WLAN Interface Board (AWL13 Compatible) Circuit Diagram is stored in the /document/hardware directory on the included DVD.

9.5.2. Interface Layout

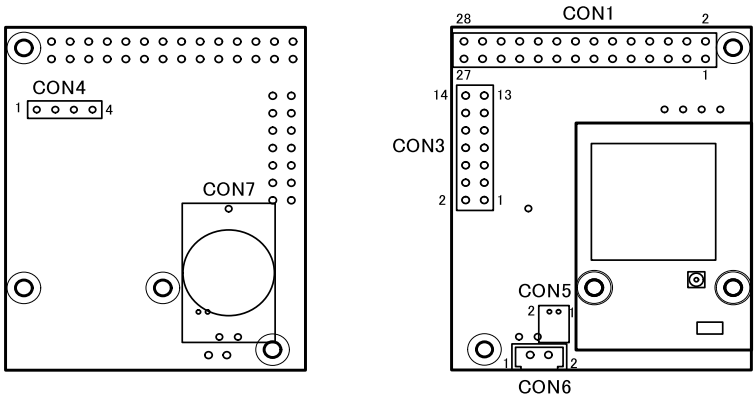


Figure 9.27. WLAN Option Module (AWL13 Compatible) Interface Layout

Table 9.18. WLAN Option Module (AWL13 Compatible) Interface Details

Symbol	Interface	Shape	Notes
CON1	Armadillo-400 Series connection	Pin socket (28P) (2.54mm pitch)	

Symbol	Interface	Shape	Notes
CON3	GPIO, UART	Pin headers (14P) (2.54mm pitch)	Connector not mounted
CON4	I2C	Pin headers (4P) (2.54mm pitch)	Connector not mounted
CON5	RTC external backup power in 1	Pin headers (2P) (1.25mm pitch) DF13-2P-1.25DS (20) (Hirose Electric)	Supported battery: CR2032 WK11 (Hitachi Maxell)
CON6	RTC external backup power in 2	Pin headers (2P) (2.54mm pitch)	Connector not mounted
CON7	RTC external backup power in 3	Battery holder HU1220 (Takachi Electronics Enclosure)	Connector not mounted, compatible batteries: CR1220 or BR1220

9.5.2.1. CON1 Armadillo-400 Series Connection Connector

This connector is for connecting to the Armadillo-400 Series Expansion Interface (CON9, CON14).

Table 9.19. WLAN Option Module (AWL13 Compatible) CON1 Signals

Pin Number	Signal Name	I/O	Function
1	+3.3V_IO	Power	Power (+3.3V_IO)
2	GND	Power	Power (GND)
3	I2C2_SCL	In	I2C Clock Connected to CON4 (pin 3) on WLAN Option Module (AWL13 Compatible)
4	I2C2_SDA	In/Out	I2C Data Connected to CON4 (pin 4) on WLAN Option Module (AWL13 Compatible)
5	SD_PWREN*	In	SD Power Enable Signal (0:ON, 1:OFF)
6	RTC_INT1*	Out	RTC Interrupt Signal
7	GPIO1_14	In/Out	General Purpose GPIO Connected to CON3 (pin 3) on WLAN Option Module (AWL13 Compatible)
8	UART5_RXD	Out	UART Data Receive Connected to CON3 (pin 4) on WLAN Option Module (AWL13 Compatible)
9	GPIO1_15	In/Out	General Purpose GPIO Connected to CON3 (pin 5) on WLAN Option Module (AWL13 Compatible)
10	UART5_TXD	In	UART Data Send Connected to CON3 (pin 6) on WLAN Option Module (AWL13 Compatible)
11	+3.3V_IO	Power	Power (+3.3V_IO)
12	+3.3V_IO	Power	Power (+3.3V_IO)
13	GND	Power	Power (GND)
14	GND	Power	Power (GND)
15	GPIO1_17	In/Out	General Purpose GPIO Connected to CON3 (pin 11) on WLAN Option Module (AWL13 Compatible)
16	GPIO1_29	In/Out	General Purpose GPIO Connected to CON3 (pin 12) on WLAN Option Module (AWL13 Compatible)
17	GPIO1_18	In/Out	General Purpose GPIO Connected to CON3 (pin 13) on WLAN Option Module (AWL13 Compatible)
18	GPIO1_30	In/Out	General Purpose GPIO Connected to CON3 (pin 14) on WLAN Option Module (AWL13 Compatible)
19	SD2_WP	-	SDIO Write Protect Detect Pull-down (10kΩ resistance)
20	SD2_CMD	In/Out	SDIO Command Connected to SDCMD signal line on AWL13
21	SD2_CD*	-	SDIO Card Detect Pull-down (10kΩ resistance)
22	SD2_CLK	In	SDIO Clock Connected to SDCLK signal line on AWL13
23	GND	Power	Power (GND)

Pin Number	Signal Name	I/O	Function
24	+3.3V_IO	Power	Power (+3.3V_IO)
25	SD2_DAT0	In/Out	SDIO Data 0 Connected to SDDATA0 signal line on AWL13
26	SD2_DAT1	In/Out	SDIO Data 1 Connected to SDDATA1 signal line on AWL13
27	SD2_DAT2	In/Out	SDIO Data 2 Connected to SDDATA2 signal line on AWL13
28	SD2_DAT3	In/Out	SDIO Data 3 Connected to SDDATA3 signal line on AWL13

9.5.2.2. CON3 GPIO, UART Interface

The CON3 interface is for connecting to the GPIO and UART on the Armadillo-400 Series. A connector is not mounted.

Table 9.20. WLAN Option Module (AWL13 Compatible) CON3 Signals

Pin Number	Signal Name	I/O	Function
1	NC	-	Not connected
2	NC	-	Not connected
3	GPIO1_14	In/Out	General Purpose GPIO Connected to CON1 (pin 7) on WLAN Option Module (AWL13 Compatible)
4	UART5_RXD	In	UART Data Receive Connected to CON1 (pin 8) on WLAN Option Module (AWL13 Compatible)
5	GPIO1_15	In/Out	General Purpose GPIO Connected to CON1 (pin 9) on WLAN Option Module (AWL13 Compatible)
6	UART5_TXD	Out	UART Data Send Connected to CON1 (pin 10) on WLAN Option Module (AWL13 Compatible)
7	+3.3V_IO	Power	Power (+3.3V_IO)
8	+3.3V_IO	Power	Power (+3.3V_IO)
9	GND	Power	Power (GND)
10	GND	Power	Power (GND)
11	GPIO1_17	In/Out	General Purpose GPIO Connected to CON1 (pin 15) on WLAN Option Module (AWL13 Compatible)
12	GPIO1_29	In/Out	General Purpose GPIO Connected to CON1 (pin 16) on WLAN Option Module (AWL13 Compatible)
13	GPIO1_18	In/Out	General Purpose GPIO Connected to CON1 (pin 17) on WLAN Option Module (AWL13 Compatible)
14	GPIO1_30	In/Out	General Purpose GPIO Connected to CON1 (pin 18) on WLAN Option Module (AWL13 Compatible)

9.5.2.3. CON4 I2C Interface

The CON4 interface is for connecting to the I2C on the Armadillo-400 Series. A connector is not mounted.

Table 9.21. WLAN Option Module (AWL13 Compatible) CON4 Signals

Pin Number	Signal Name	I/O	Function
1	+3.3V_IO	Power	Power (+3.3V_IO)
2	GND	Power	Power (GND)
3	I2C2_SCL	In	I2C Clock Connected to CON1 (pin 3) on WLAN Option Module (AWL13 Compatible)
4	I2C2_SDA	Out	I2C Data Connected to CON1 (pin 4) on WLAN Option Module (AWL13 Compatible)

9.5.2.4. CON5, CON6, CON7 External Backup Connectors

These are external backup connectors for the RTC equipped on the WLAN Option Module (AWL13 Compatible). It is possible to connect a separate external battery in order to maintain time data during extended periods of no power supply.

Table 9.22. WLAN Option Module (AWL13 Compatible) CON5, CON6 Signals

Pin Number	Signal Name	I/O	Function
1	BAT	Power	RTC external backup power in
2	GND	Power	GND

As CON5, CON6 and CON7 are connected to the same terminals they cannot be used at the same time.

When connecting batteries aside from lithium coins (CR or BR) to the External RTC Backup Connectors (CON5, CON6), please ensure that they do not exceed the rated maximum values of the equipped components as shown in the "Armadillo-400 Series WLAN Interface Board (AWL13 Compatible) Circuit Diagram" stored in the /document/hardware directory on the included DVD.

9.5.3. Board Outline Diagrams

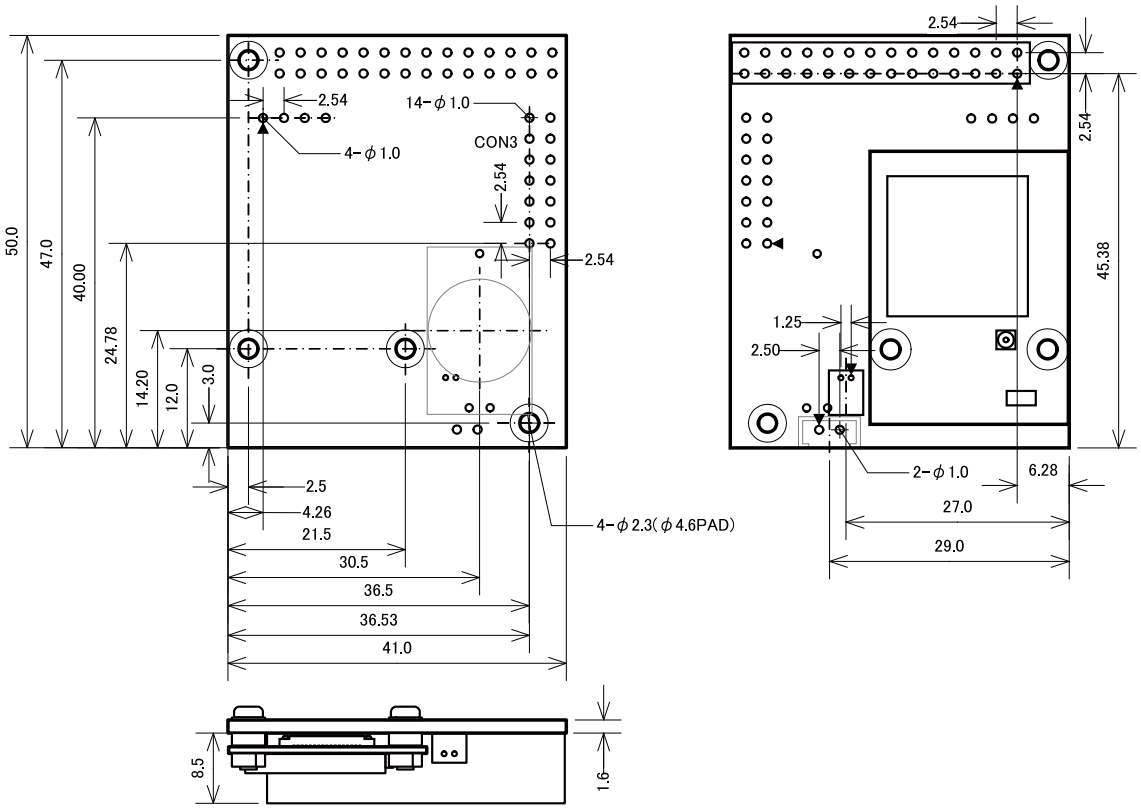


Figure 9.28. WLAN Option Module (AWL13 Compatible) Dimensions

9.5.4. Assembly

While the following describes assembly with Armadillo-420/440, the same method can be used with Armadillo-460.

9.5.4.1. AWL13 And WLAN Interface Board (AWL13 Compatible) Assembly

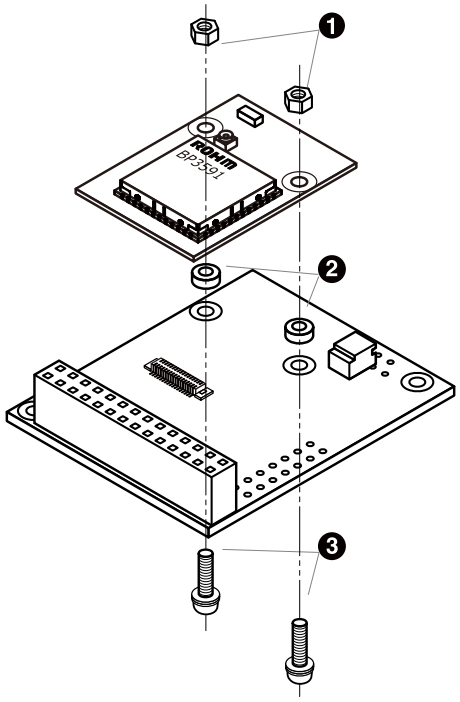


Figure 9.29. AWL13 and WLAN Interface Board (AWL13 Compatible) Assembly Diagram

1. Nut (M2, L=1.6mm, D=4mm)
2. Metal spacer (M2, L=1.5mm, D=4mm)
3. Round head screw (M2, L=8mm, spring washer + small washer)

Position the connectors on the AWL13 and WLAN Interface Board (AWL13 Compatible) together and then connect them. Please take care as applying too much force may cause damage.

9.5.4.2. WLAN Option Module (AWL13 Compatible) and Armadillo-400 Series Assembly

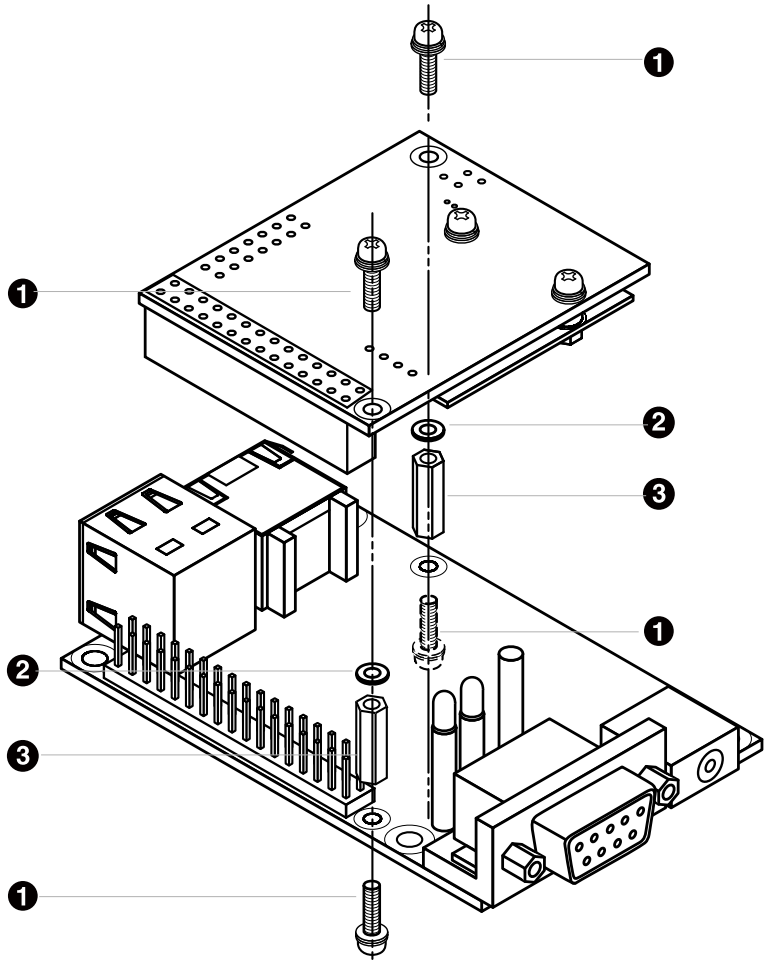


Figure 9.30. WLAN Option Module (AWL13 Compatible) and Armadillo-400 Series Assembly Diagram

1. Round head screw (M2, L=6mm, spring washer + small washer)
2. Metal spacer (M2, L=11mm, D=4mm)
3. Washer (M2, L=0.3mm, D=4.3mm)

9.5.4.3. WLAN Option Module (AWL13 Compatible) And External Antenna Assembly (For Evaluation and Development)

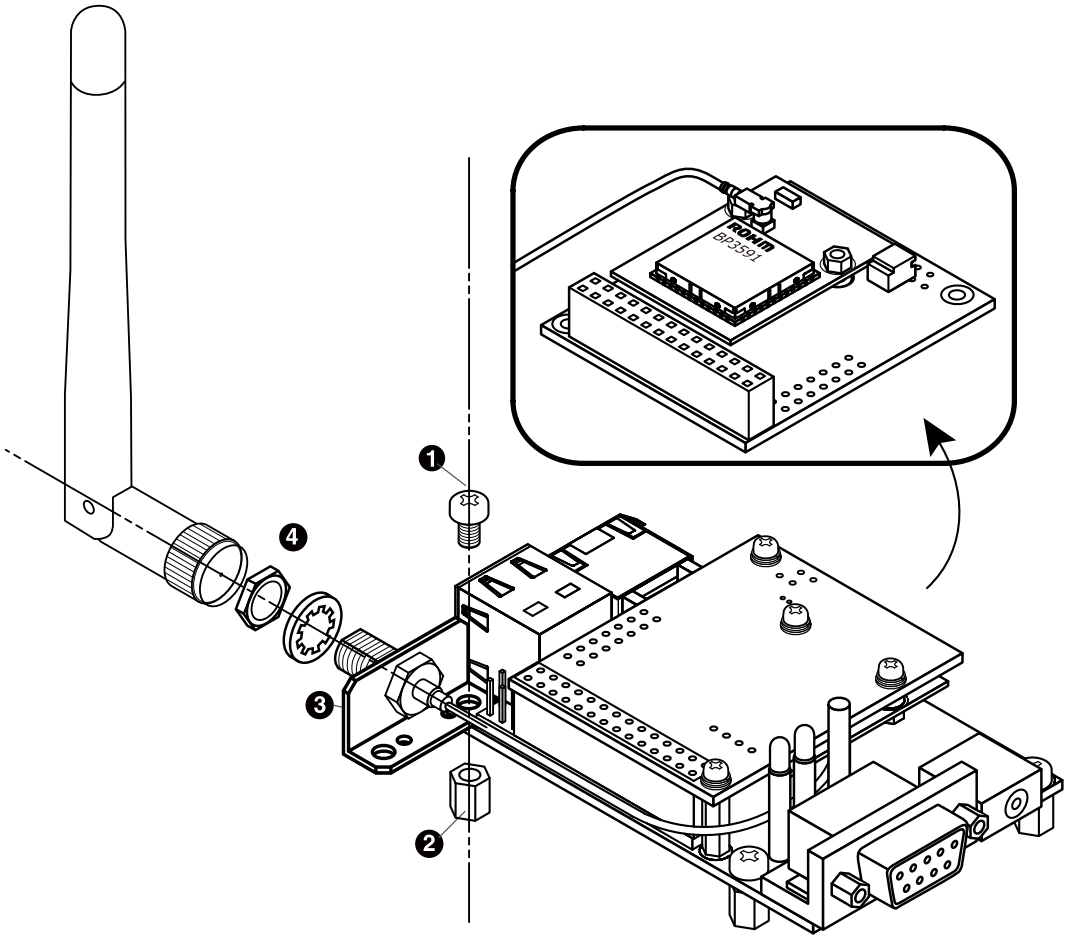


Figure 9.31. WLAN Option Module (AWL13 Compatible) and External Antenna Assembly Diagram (For Evaluation and Development)

1. Round head screw (M3, L=5mm)
2. Plastic spacer (M3, L=8mm, D=5.5mm)
3. External Antenna Metal Fitting
4. External Antenna

When connecting the external antenna cable to the antenna terminal on the AWL13, please be careful not to apply too much force as it may cause damage.

When removing the external antenna cable, it is recommended to use a dedicated removal tool (U.FL-LP-N-2 Hirose Electric). Doing so without a dedicated removal tool may cause the connector to deform or the cable to break.

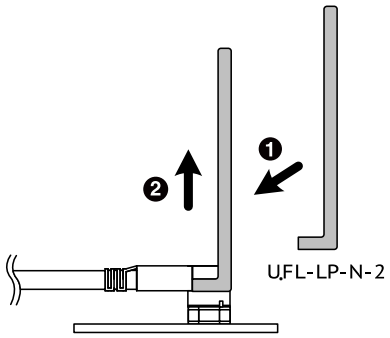


Figure 9.32. External Antenna Cable Removal

If an external antenna cable is connected to the antenna terminal on the AWL13 for an extended period of time, the switch in the coaxial connector may not return. If it does not return, the chip antenna will no longer be usable.

During evaluation and development, when not using the WLAN Option Module (AWL13 Compatible) for a long period of time please store it after having removed the external antenna cable from the antenna terminal on the AWL13. Also, when employing the WLAN Option Module (AWL13 Compatible) as part of a mass produced product, it is not recommended to switch from the external antenna to the chip antenna connection.

Chapter 10. Case

The following provides details on the Armadillo-400 Series Option Case.

10.1. Plastic Case (Product ID: OP-CASE400-PLA-00)

The Armadillo-400 Series Option Case (Plastic) is a small plastic case for Armadillo-420/440. When Armadillo-420/440 are placed in the case, the DC jack, serial interface (D-Sub 9 pin), USB interface, and LAN interface are accessible. The case also has a removable cover to provide an opening for accessing CON9 (Expansion Interface 1).

The plastic case is included in the Armadillo-420 Basic Model Development Set and is also available for sale separately.

Table 10.1. Armadillo-400 Series Option Case (Plastic) Details

Product Name	Armadillo-400 Series Option Case (Plastic)
Product Number	OP-CASE400-PLA-00
Contents	Plastic case, screws and rubber feet

Table 10.2. Plastic Case Material Specifications

Product Number	VA55
Grade	Flame resistant (standard general)
Halogen	Halogen variety
UL94	V-0.5V
Temperature Index (max usable temperature)	60℃

If the plastic case is used or stored at a temperature higher than the maximum usable temperature, there is a possibility that it will deform.

Please note that it cannot be used with Armadillo-460.

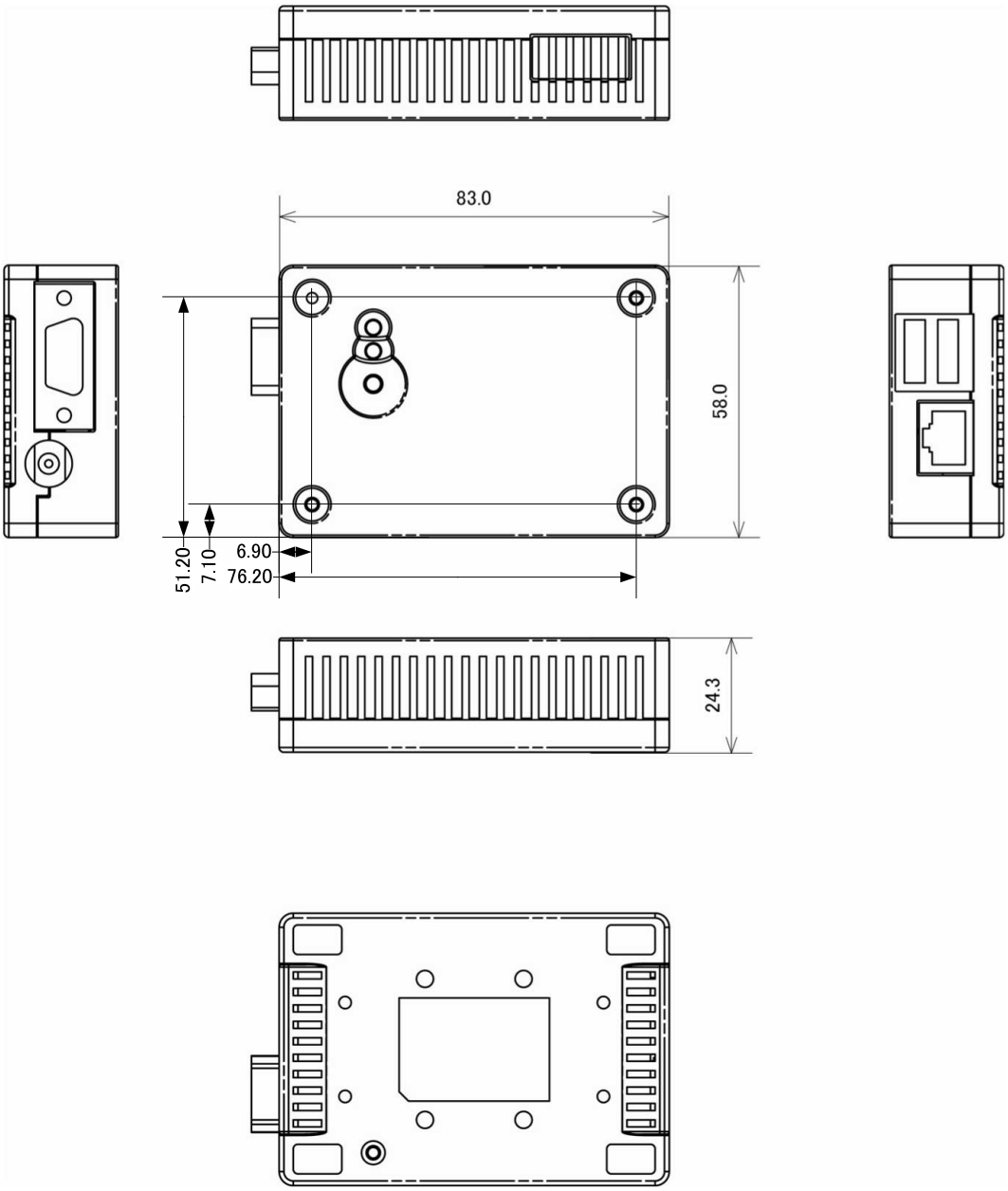


Figure 10.1. Plastic Case Dimensions (mm)

10.2. Plastic Case (Product ID: OP-CASE400-MET-00)

The Armadillo-400 Series Option Case (Metal) is a small aluminum case. When the board is placed in the case, the DC jack, serial interface (D-Sub 9 pin), USB interface, and LAN interface are accessible. Also, parts for fixing the AC adapter cable and an earth line can be connected by using the case fixing screws.

The metal case is sold separately as an option.

Please note that it cannot be used with Armadillo-460.

Table 10.3. Armadillo-400 Series Option Case (Metal) Details

Product Name	Armadillo-400 Series Option Case (Metal)
Product Number	OP-CASE400-MET-00
Contents	Aluminum case, screws, rubber feet, AC adapter cable fixing parts

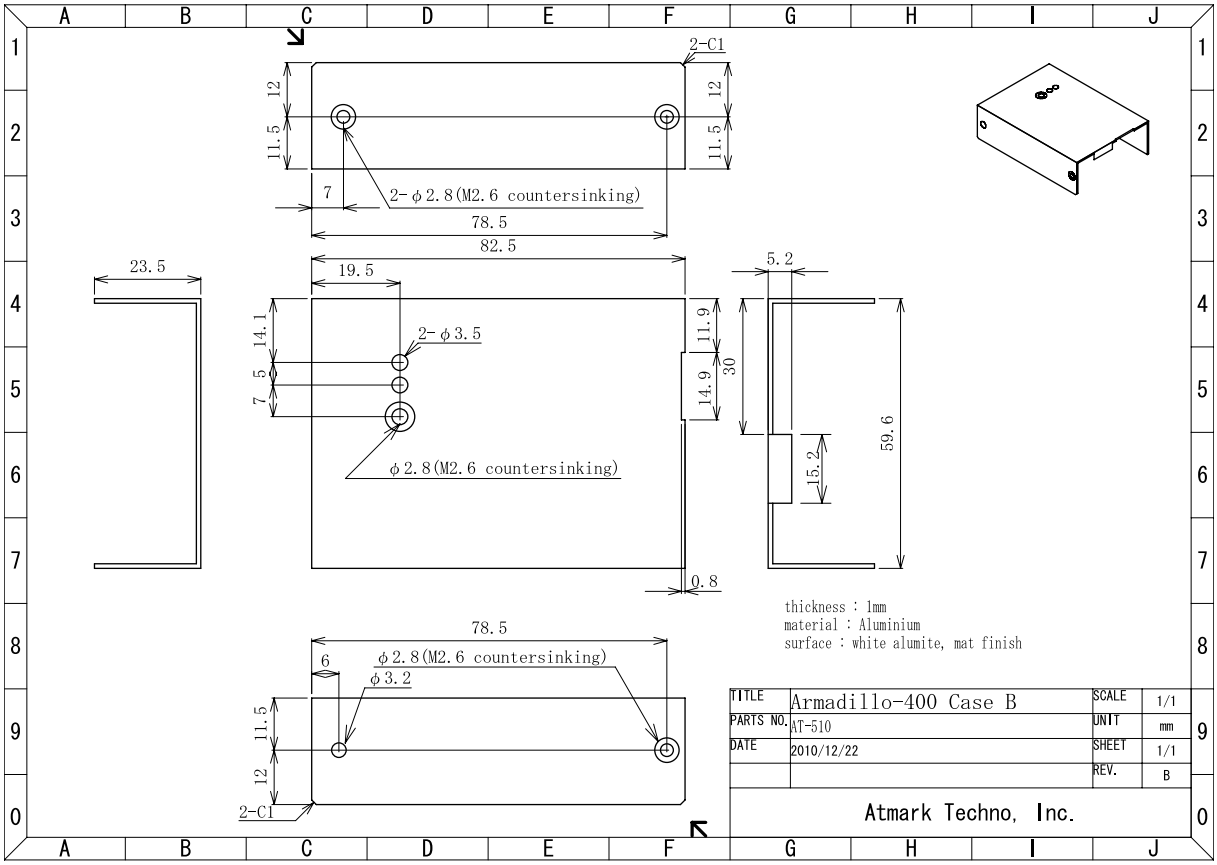


Figure 10.2. Metal Case (Upper Plate) Dimensions

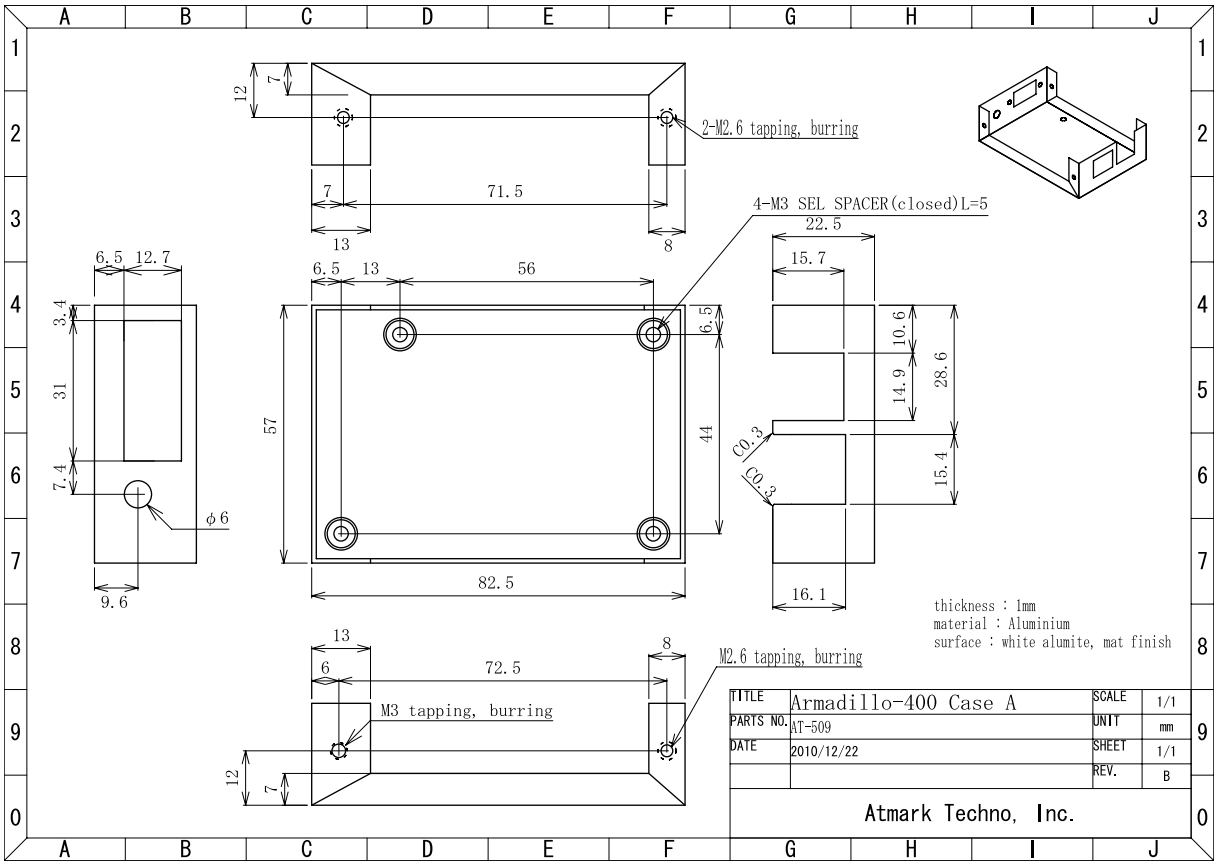


Figure 10.3. Metal Case (Lower Plate) Dimensions

As aluminum has good workability characteristics, customization like adding holes is possible.

The following is a reference diagram for when attaching the external antenna of Armadillo-WLAN. The DXF file (version: AC1015) of the reference diagram is stored in the /document/case directory on the included DVD.

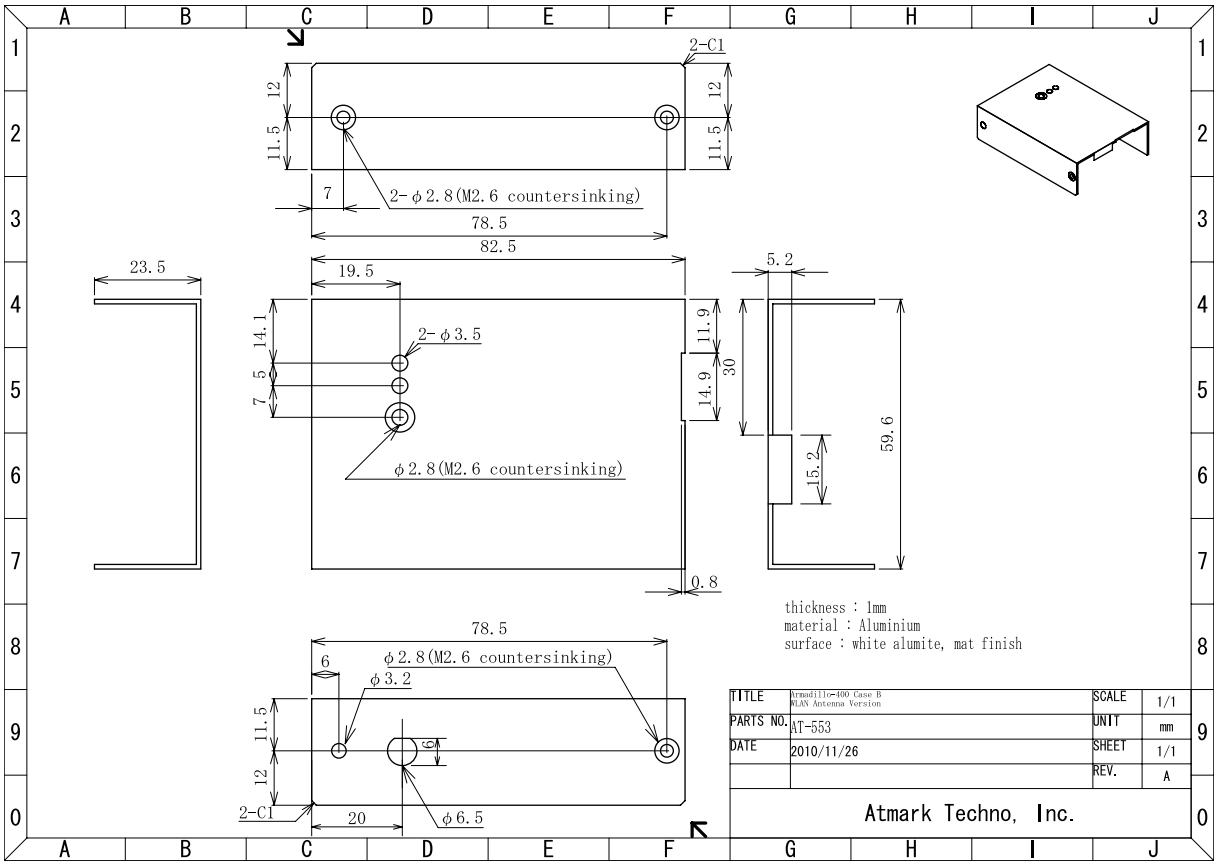


Figure 10.4. Metal Case (Upper Plate) Customization Example (Armadillo-WLAN External Antenna Dimensions)

Appendix A. Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00)

The Armadillo-400 Series option "Armadillo-400 Series JTAG Conversion Cable" (OP-JC8P25-00) is used to convert the i.MX257 JTAG Interface (CON10) on the Armadillo-400 Series to the standard ARM connector (20 pin, 2.54mm pitch).

A connection diagram and reference circuit for the JTAG Conversion Cable are shown below.

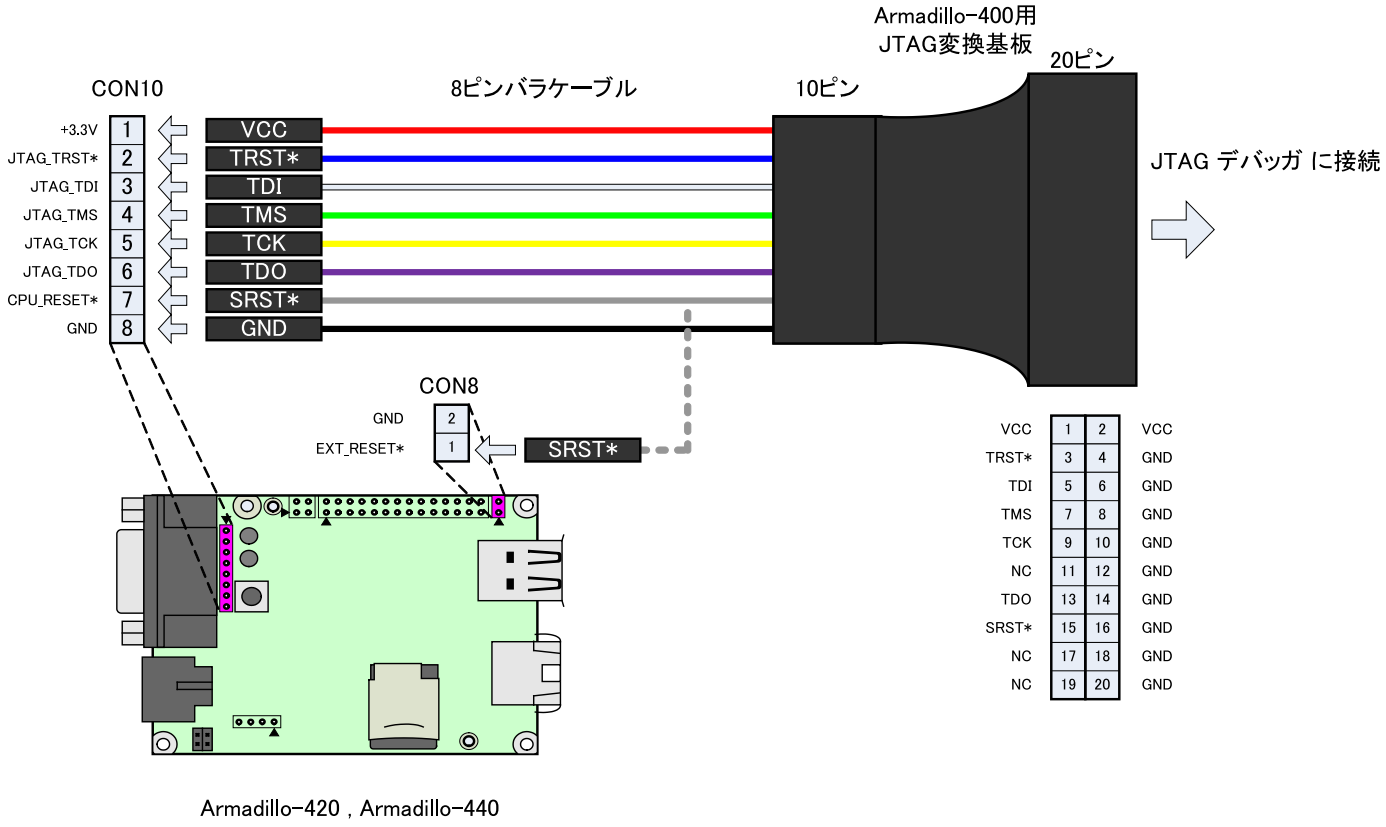


Figure A.1. JTAG Conversion Cable Connection Diagram (Armadillo-420,Armadillo-440)

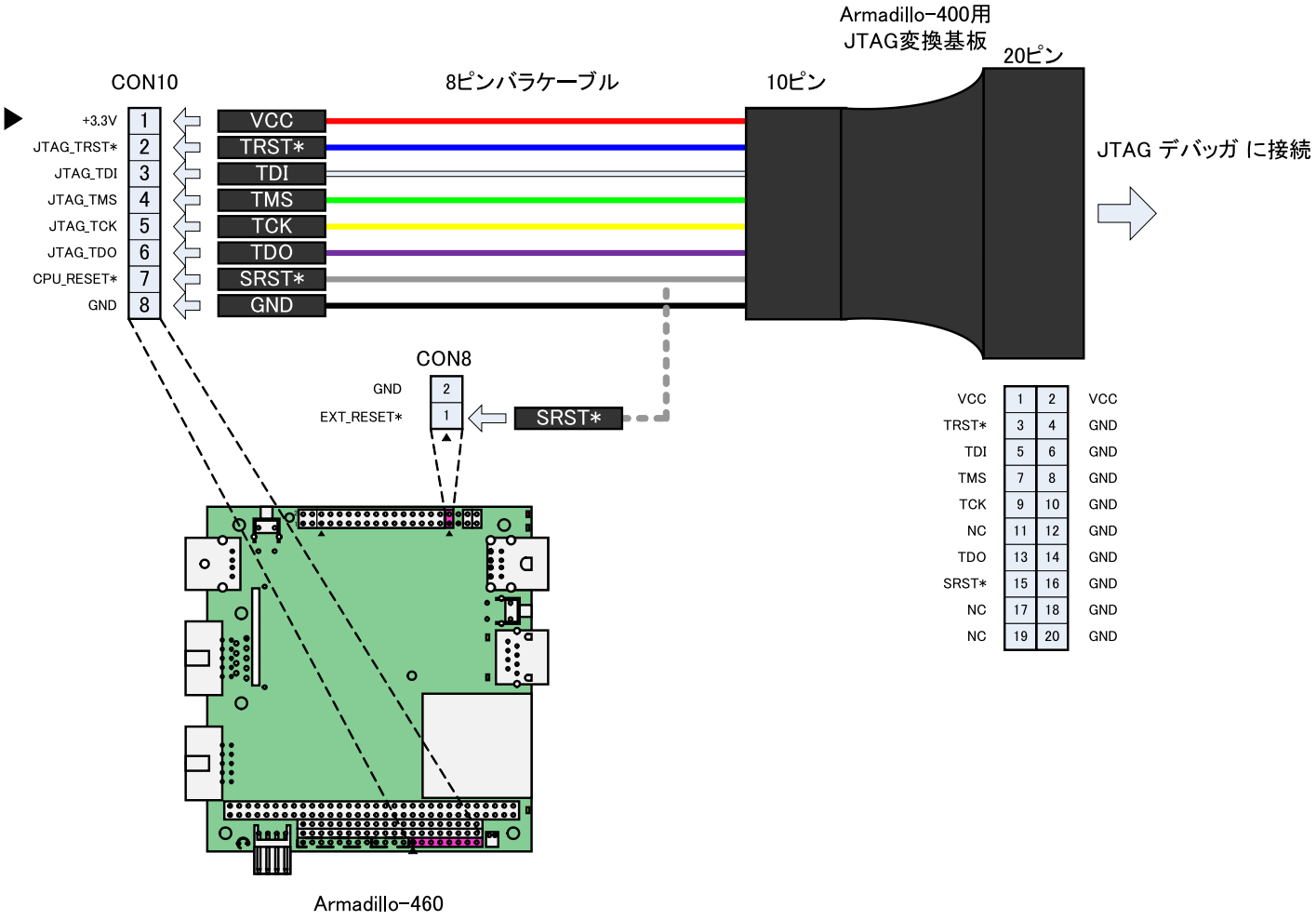


Figure A.2. JTAG Conversion Cable Connection Diagram (Armadillo-460)

When the SRST* signal on the JTAG Conversion Cable is connected to the CPU_RESET* pin on CON10, only i.MX257 is reset. To reset the full board using a JTAG debugger, please connect the SRST* signal to the EXT_RESET* pin on CON8.

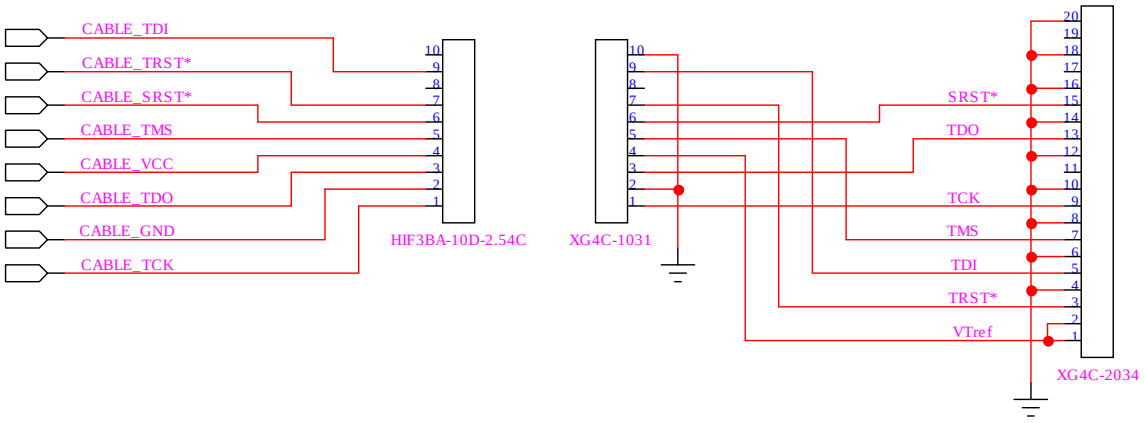


Figure A.3. JTAG Conversion Cable Reference Circuit

Appendix B. Initial Configuration State of Expansion Interfaces

The initial states of the signal pins and pad configuration of the CON9, CON11 (Armadillo-440, Armadillo-460) and CON14 expansion interfaces on the Armadillo-400 Series are shown below.

Table B.1. Signal State of Expansion Interfaces (After i.MX257 Reset)

Connector	Pin Number	Signal Name	Signal State After Reset				On-board Pull-up
			I/O	Pin State	Open Drain	Pull/Keeper	
CON14	3	EXT_IO22	In	-	Disable	100kΩPD[a]	-
	4	EXT_IO23	In	-	Disable	Disable	-
CON9	1	EXT_IO0	Out	Low	Disable	Disable	-
	2	EXT_IO1	Out	Low	Disable	Disable	-
	3	EXT_IO2	In	-	Disable	100kΩPU[a]	-
	4	EXT_IO3	In	-	Disable	Keeper	-
	5	EXT_IO4	Out	Low	Disable	100kΩPU	-
	6	EXT_IO5	In	-	Disable	Keeper	-
	11	EXT_IO6	In	-	Disable	100kΩPU	-
	12	EXT_IO7	In	-	Disable	Keeper	-
	13	EXT_IO8	In	-	Disable	100kΩPU	-
	14	EXT_IO9	In	-	Disable	Keeper	-
	15	EXT_IO10	In	-	Disable	Keeper	-
	16	EXT_IO11	In	-	Disable	Keeper	-
	17	EXT_IO12	In	-	Disable	Keeper	-
	18	EXT_IO13	In	-	Disable	Keeper	-
	21	EXT_IO14	Out	Low	Disable	Disable	-
	22	EXT_IO15	In	-	Disable	Keeper	-
	23	EXT_IO16	In	-	Disable	Keeper	-
	24	EXT_IO17	In	-	Disable	Keeper	-
	25	EXT_IO18	In	-	Disable	100kΩPU	-
	26	EXT_IO19	In	-	Disable	100kΩPU	-
	27	EXT_IO20	Out	Undefined	Disable	Disable	-
	28	EXT_IO21	In	-	Disable	Disable	-

Connector	Pin Number	Signal Name	Signal State After Reset				On-board Pull-up
			I/O	Pin State	Open Drain	Pull/Keeper	
CON11	8	LCD_LSCLK	Out	Low	Disable	Disable	47kΩPD[b]
	9	LCD_HSYN	Out	Low	Disable	Disable	47kΩPD[b]
	10	LCD_VSYN	Out	Low	Disable	Disable	47kΩPD[b]
	11	LCD_OE_ACD	Out	Low	Disable	Disable	47kΩPD[b]
	12	PWMO1	In	-	Disable	100kΩPD	47kΩPD[b]
	13	LCD_LD0	Out	Low	Disable	Disable	47kΩPD[b]
	14	LCD_LD1	Out	Low	Disable	Disable	47kΩPD[b]
	15	LCD_LD2	Out	Low	Disable	Disable	47kΩPD[b]
	16	LCD_LD3	Out	Low	Disable	Disable	47kΩPD[b]
	17	LCD_LD4	Out	Low	Disable	Disable	47kΩPD[b]
	18	LCD_LD5	Out	Low	Disable	Disable	47kΩPD[b]
	20	LCD_LD6	Out	Low	Disable	Disable	47kΩPU
	21	LCD_LD7	Out	Low	Disable	Disable	47kΩPD[b]
	22	LCD_LD8	Out	Low	Disable	Disable	47kΩPD[b]
	23	LCD_LD9	Out	Low	Disable	Disable	47kΩPD[b]
	24	LCD_LD10	Out	Low	Disable	Disable	47kΩPD[b]
	25	LCD_LD11	Out	Low	Disable	Disable	47kΩPD[b]
	27	LCD_LD12	Out	Low	Disable	Disable	47kΩPD[b]
	28	LCD_LD13	Out	Low	Disable	Disable	47kΩPD[b]
	29	LCD_LD14	Out	Low	Disable	Disable	47kΩPU
	30	LCD_LD15	Out	Low	Disable	Disable	47kΩPU
	31	LCD_LD16	In	-	Enable	100kΩPU	-
	32	LCD_LD17	In	-	Disable	Disable	-
	39	EXT_IO24	In	-	Disable	47kΩPU	-
	40	EXT_IO25	In	-	Disable	100kΩPU	-
	41	EXT_IO26	In	-	Disable	100kΩPU	-
	42	EXT_IO27	In	-	Disable	100kΩPU	-
	43	EXT_IO28	In	-	Disable	100kΩPU	-
	44	EXT_IO29	In	-	Enable	100kΩPU	-
	45	EXT_IO30	In	-	Enable	100kΩPU	-
	46	EXT_IO31	In	-	Enable	100kΩPU	-
	47	EXT_IO32	In	-	Enable	100kΩPU	-
	48	EXT_IO33	In	-	Disable	Disable	-
	49	EXT_IO34	In	-	Disable	100kΩPD	-

[a]PD=Pull Down, PU=Pull Up

[b]Open on Armadillo-460

Table B.2. Signal State of Expansion Interfaces (After Bootloader Configuration)

Connec-tor	Pin Number	Signal Name	Signal State After Bootloader Boot[a]					
			Mux Mode	I/O	Pin State	Open Drain	Pull/Keeper	Slew Rate
CON14	3	EXT_IO22	GPIO	In	-	Disable	100kΩPU	Slow
	4	EXT_IO23	GPIO	In	-	Disable	100kΩPU	Slow

Connec-tor	Pin Number	Signal Name	Signal State After Bootloader Boot[a]					
			Mux Mode	I/O	Pin State	Open Drain	Pull/Keeper	Slew Rate
CON9	1	EXT_IO0	GPIO	In	-	Disable	100kΩPU	Slow
	2	EXT_IO1	GPIO	In	-	Disable	100kΩPU	Slow
	3	EXT_IO2	GPIO	In	-	Disable	100kΩPU	Slow
	4	EXT_IO3	GPIO	In	-	Disable	100kΩPU	Slow
	5	EXT_IO4	GPIO	In	-	Disable	100kΩPU	Slow
	6	EXT_IO5	GPIO	In	-	Disable	100kΩPU	Slow
	11	EXT_IO6	GPIO	In	-	Disable	100kΩPU	Slow
	12	EXT_IO7	GPIO	In	-	Disable	100kΩPU	Slow
	13	EXT_IO8	GPIO	In	-	Disable	100kΩPU	Slow
	14	EXT_IO9	GPIO	In	-	Disable	100kΩPU	Slow
	15	EXT_IO10	GPIO	In	-	Disable	100kΩPU	Slow
	16	EXT_IO11	GPIO	In	-	Disable	100kΩPU	Slow
	17	EXT_IO12	GPIO	In	-	Disable	100kΩPU	Slow
	18	EXT_IO13	GPIO	In	-	Disable	100kΩPU	Slow
	21	EXT_IO14	GPIO	In	-	Disable	100kΩPU	Slow
	22	EXT_IO15	GPIO	In	-	Disable	100kΩPU	Slow
	23	EXT_IO16	GPIO	In	-	Disable	100kΩPU	Slow
	24	EXT_IO17	GPIO	In	-	Disable	100kΩPU	Slow
	25	EXT_IO18	GPIO	In	-	Disable	100kΩPU	Slow
	26	EXT_IO19	GPIO	In	-	Disable	100kΩPU	Slow
	27	EXT_IO20	GPIO	Out	Low	Disable	Disable	Fast
	28	EXT_IO21	GPIO	Out	Low	Disable	Disable	Fast

Connec-tor	Pin Number	Signal Name	Signal State After Bootloader Boot[a]					
			Mux Mode	I/O	Pin State	Open Drain	Pull/Keeper	Slew Rate
CON11	8	LCD_LSCLK	LCD	Out	Low	Disable	Disable	Fast
	9	LCD_HSYN	LCD	Out	Low	Disable	Disable	Slow
	10	LCD_VSYN	LCD	Out	Low	Disable	Disable	Slow
	11	LCD_OE_ACD	LCD	Out	Low	Disable	Disable	Slow
	12	PWMO1	PWMO1	Out	Low	Disable	100kΩPU	Slow
	13	LCD_LD0	LCD	Out	Low	Disable	Disable	Slow
	14	LCD_LD1	LCD	Out	Low	Disable	Disable	Slow
	15	LCD_LD2	LCD	Out	Low	Disable	Disable	Slow
	16	LCD_LD3	LCD	Out	Low	Disable	Disable	Slow
	17	LCD_LD4	LCD	Out	Low	Disable	Disable	Slow
	18	LCD_LD5	LCD	Out	Low	Disable	Disable	Slow
	20	LCD_LD6	LCD	Out	Low	Disable	Disable	Slow
	21	LCD_LD7	LCD	Out	Low	Disable	Disable	Slow
	22	LCD_LD8	LCD	Out	Low	Disable	Disable	Slow
	23	LCD_LD9	LCD	Out	Low	Disable	Disable	Slow
	24	LCD_LD10	LCD	Out	Low	Disable	Disable	Slow
	25	LCD_LD11	LCD	Out	Low	Disable	Disable	Slow
	27	LCD_LD12	LCD	Out	Low	Disable	Disable	Slow
	28	LCD_LD13	LCD	Out	Low	Disable	Disable	Slow
	29	LCD_LD14	LCD	Out	Low	Disable	Disable	Slow
	30	LCD_LD15	LCD	Out	Low	Disable	Disable	Slow
	31	LCD_LD16	LCD	Out	Low	Disable	100kΩPU	Slow
	32	LCD_LD17	LCD	Out	Low	Disable	100kΩPU	Slow
	39	EXT_IO24	GPIO	In	-	Disable	47kΩPU	Slow
	40	EXT_IO25	GPIO	In	-	Disable	100kΩPU	Slow
	41	EXT_IO26	GPIO	In	-	Disable	100kΩPU	Slow
	42	EXT_IO27	GPIO	In	-	Disable	100kΩPU	Slow
	43	EXT_IO28	GPIO	In	-	Disable	100kΩPU	Slow
	44	EXT_IO29	GPIO	In	-	Disable	100kΩPU	Slow
	45	EXT_IO30	GPIO	In	-	Disable	100kΩPU	Slow
	46	EXT_IO31	GPIO	In	-	Disable	100kΩPU	Slow
	47	EXT_IO32	GPIO	In	-	Disable	100kΩPU	Slow
	48	EXT_IO33	GPIO	In	-	Disable	100kΩPU	Slow
	49	EXT_IO34	GPIO	In	-	Disable	100kΩPU	Slow

[a]Current output set to "Std" on all signals.

Appendix C. Connector Information

Connector mount information for the Armadillo-400 Series development sets (A4xxx-DxxZ) and mass production boards (A4xxx-UxxZ) is shown in Table C.2, “Connector Product Numbers List”. Also, the meanings of the symbols used in Table C.2, “Connector Product Numbers List” are shown in Table C.1, “Table C.2, “Connector Product Numbers List” Symbols”. For connector mount information on Armadillo-400 Series mass production boards (A4xxx-BxxZ), please contact us from our web site[1].

Table C.1. Table C.2, “Connector Product Numbers List” Symbols

Symbol	Symbol Meaning
○	Connector mounted as standard
△	Connector not mounted but can be as an option
/	Connector not an option
-	No recommendation for connector

[1] http://www.atmark-techno.com/contactinfo/

Table C.2. Connector Product Numbers List

Part Number	Interface	Shape	Equipped As Standard			Board Side Connector		Corresponding Connector (Reference)	
			420	440	460	Product Number	Maker	Product Number	Maker
CON1	SD	microSD slot	○	○	/	DM3C-SF	HIROSE	-	-
		SD slot	/	/	○	CIM-H81N	MITSUMI	-	-
CON2	LAN	RJ-45 Connector	○	○	○	TM11R-5M2-88-LP	HIROSE	-	-
CON3	Serial	D-Sub 9 pin	○	○	△	DEL09PBTK1YS-F	GTK	-	-
CON4	Serial	Pin headers (10P) (2.54mm pitch)	△	△	△	A1-10PA-2.54DSA(71)	HIROSE	A1-10D-2.54C	HIROSE
			△	△	○	XG4C-1034	OMRON	XG4T-1004 + XG4M-1030 + XG5Z-0002	OMRON
			△	△	△	XG8B-0134	OMRON	XG4T-1004 + XG4M-1030 + XG5Z-0002	OMRON
CON5	USB	Type-A connector	○	○	△	UBA-4RS-D14T-4D(LF)(SN)	JST	-	-
		Type-A connector	△	△	○	UBA-4RS-D14T-4D (LF)(SN)			
CON6	USB	Pin headers (4P) (2mm pitch)	△	△	/	MTMM-104-09-L-S-365	SAMTEC	-	-
		Pin headers (4P) (2mm pitch)	△	△	/	B4B-PH-K-S(LF)(SN)	JST	PHR-4	JST
		Pin headers (4P) (2.54mm pitch)	/	/	△	A2-4PA-2.54DSA(71)	HIROSE	RE-04	JST
CON7	LAN	Pin headers (10P) (2.54mm pitch)	△	△	△	A1-10PA-2.54DSA(71)	HIROSE	A1-10D-2.54C	HIROSE
			△	△	/	XG8B-0134	OMRON	XG4T-1004 + XG4M-1030 + XG5Z-0002	OMRON
			△	△	/	XG4C-1034	OMRON	XG4T-1004 + XG4M-1030 + XG5Z-0002	OMRON
CON8	External Reset	Pin headers (2P) (2.54mm pitch)	○	○	○	A1-34PA-2.54DSA(71)	HIROSE	RE-02	JST
CON9	Expansion	Pin headers (28P) (2.54mm pitch)	○	○	○			RF-28	JST
CON14	Expansion	Pin headers (4P) (2.54mm pitch)	○	○	○			PS-4SLA-D4C2	JAE

Part Number	Interface	Shape	Equipped As Standard			Board Side Connector		Corresponding Connector (Reference)	
			420	440	460	Product Number	Maker	Product Number	Maker
CON8	External Reset	Pin headers (2P) (2.54mm pitch)	△	△	△	XG8B-0134 (34pin)	OMRON	XG4T-3404 + XG4M-3430 + XG5Z-0002	OMRON
CON9	Expansion	Pin headers (28P) (2.54mm pitch)	△	△	△				
CON14	Expansion	Pin headers (4P) (2.54mm pitch)	△	△	△				
CON10	i.MX257 JTAG	Pin headers (8P) (2.54mm pitch)	○	○	○	A2-8PA-2.54DSA(71)	HIROSE	RE-08	JST
CON11	LCD Expansion	FFC Connector (50P) (0.5mm pitch)	/	○	○	XF2M-5015-1A	OMRON	-	-
CON12	Power in	DC jack	○	○	/	HEC3690-015210	HOSHIDEN	-	-
		Pin headers (4P) (2.5mm pitch)	/	/	○	171826-4	TYCO	-	-
CON13	Power in	Pin headers (4P) (2.54mm pitch)	△	△	/	A2-4PA-2.54DSA(71)	HIROSE	RE-04	JST
		Pin headers (3P) (2.54mm pitch)	△	△	/	171826-3	TYCO	171822-3	TYCO
		Pin headers (8P) (2.54mm pitch)	/	/	△	A2-8PA-2.54DSA(71)	HIROSE	RE-08	JST
CON17	USB	Type-A connector	/	/	○	UBA-4RS-D14T-4D (LF) (SN)	JST	-	-
CON18	USB	Pin headers (4P) (2.54mm pitch)	/	/	△	A2-4PA-2.54DSA(71)	HIROSE	RE-04	JST
CON19	Serial	Pin headers (10P) (2.54mm pitch)	/	/	○	XG4C-1034	OMRON	XG4U-1004 + XG4M-1030	OMRON
CON20	RTC external backup power	Pin headers (2P) (1.25mm pitch)	/	/	○	DF13-2P-1.25DS (20)	HIROSE	DF13-2S-1.25C	HIROSE
CON21	Power Out	Pin headers (4P) (2.54mm pitch)	/	/	△	A2-4PA-2.54DSA(71)	HIROSE	RE-04	JST
CON22	User switch	Pin headers (6P) (2.54mm pitch)	/	/	△	A1-6PA-2.54DSA (71)	HIROSE	RF-06	JST
CON23	SD	Pin headers (10P) (2.54mm pitch)	/	/	△	XG4C-1034	OMRON	XG4T-1004 + XG4M-1030	OMRON
CON24	Reserved	Reserved	/	/	△	Reserved	Reserved	Reserved	Reserved
CON25	SD	Pin headers (10P) (2.54mm pitch)	/	/	△	95278-101A10LF	FCI	XG4T-1030 + XG4M-1030	OMRON

Part Number	Interface	Shape	Equipped As Standard			Board Side Connector		Corresponding Connector (Reference)	
			420	440	460	Product Number	Maker	Product Number	Maker
J1	Expansion Bus	Pin headers (64P) (2.54mm pitch)	/	/	Yes	25-0206-232-1G-R	ASTRON	-	-
J2	Expansion Bus	Pin headers (20P) (2.54mm pitch)	/	/	Yes	1150020-004-R	ASTRON	-	-
LED3	User LED	LED (red) (ϕ3mm)	○	○	/	OSDR3133A / LK-12	OPTO SUPPLY / MAC8	-	-
LED4	User LED	LED (green) (ϕ3mm)	○	○	/	OSNG3133A / LK-12	OPTO SUPPLY / MAC8	-	-
SW1	User switch	Tact Switch (h=17mm)	○	○	△	SKHHDJA010	ALPS	-	-
		Tact Switch (l=4.3mm)	△	△	△	SKHHALA010	ALPS	-	-
		Tact Switch (l=3.3mm)	/	/	○	SKHHLUA010	ALPS	-	-
SW2	Reset Switch	Tact Switch (l=3.3mm)	/	/	○	SKHHLUA010	ALPS	-	-
SW3	User switch	Tact Switch (h=7mm)	/	/	△	SKHHBVA010	ALPS	-	-
SW4	Reset Switch	Tact Switch (h=7mm)	/	/	△	SKHHBVA010	ALPS	-	-
JP1	Boot mode jumper	Pin headers (2P) (2.54mm pitch)	Yes	Yes	○	A1-34PA-2.54DSA(71)	HIROSE	881545-2	AMP
JP2	User jumper	Pin headers (2P) (2.54mm pitch)	Yes	Yes	○				

Appendix D. Resistor Information - Armadillo-460

The following selections are possible on Armadillo-460 by making changes to the mounted chip resistors (0Ω).

- PC/104 Expansion Bus Power V_PC104 Selection
- USB Full Speed Signal Output Connector Selection

Table D.1. PC/104 Expansion Bus Power V_PC104 Selection

V_PC104	Resistor	Chip Resistor Size
VIN	Mount chip resistor (0Ω) at R271 (standard)	2.0 x 1.2 mm
+3.3V_EXT	Mount chip resistor (0Ω) at R270	

Either VIN (+5V) or +3.3V_EXT (+3.3V) can be selected for PC/104 Expansion Bus power V_PC104.

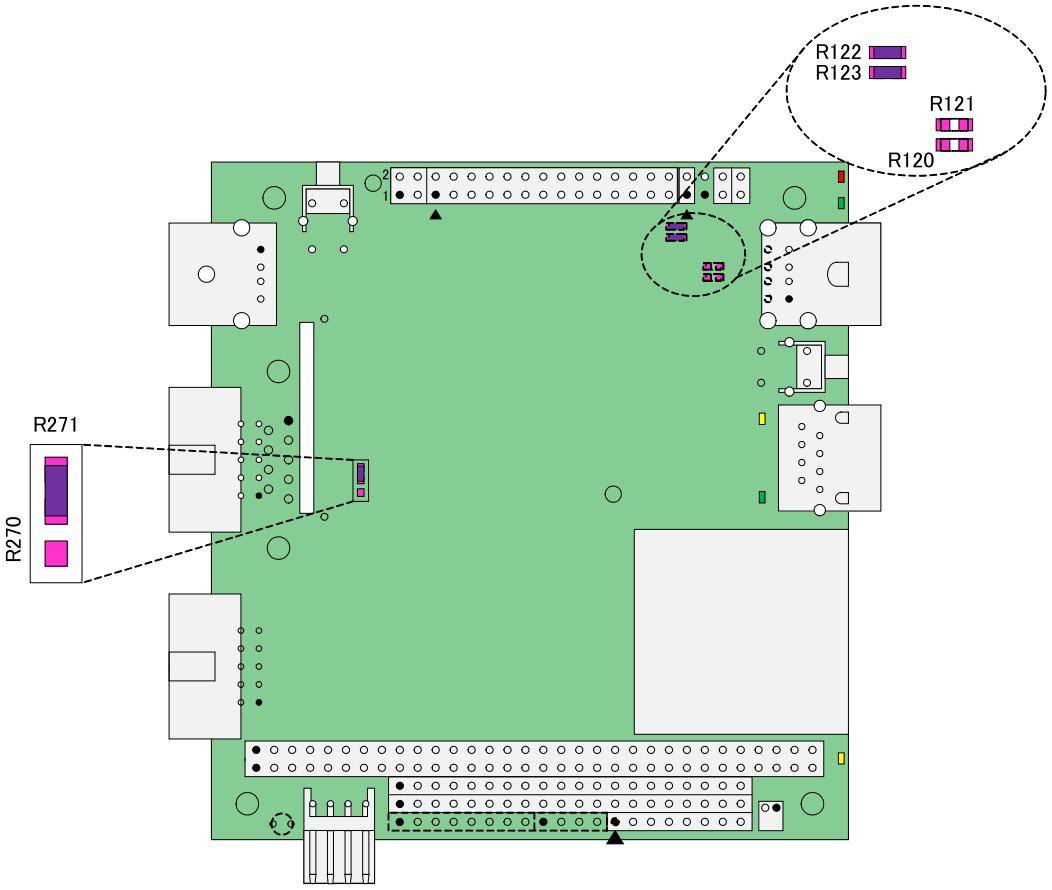
Please mount to only one of R271 and R270 as mounting both will cause VIN and +3.3V_EXT to short and cause damage.

Table D.2. USB Full Speed Signal Output Connector Selection

USB Full Speed	Resistor	Chip Resistor Size
CON17,CON18	Mount chip resistors (0Ω) at R122 and R123 (standard)	1.6 x 0.8 mm
CON5 (upper)	Mount chip resistors (0Ω) at R120 and R121	

Please only mount chip resistors to one of the R122/123 and R120/121 sets.

The resistor positions on Armadillo-460 are shown below.



Armadillo-460(表面)

Figure D.1. Armadillo-460 Resistor Information

Please take care when changing resistors as they may short on the board.

Appendix E. CPLD Registers - Armadillo-460

E.1. CPLD Register Memory Map

The memory map of the CPLD register is as shown.

Table E.1. CPLD Register Memory Map

Address	Name	Description	Access
0xA800 0000	Ext Interrupt Status0	Expansion Bus Interrupt Status Register 0	Read/Write
0xA800 0001	Ext Interrupt Status1	Expansion Bus Interrupt Status Register 1	Read/Write
0xA800 0002	Ext Interrupt Mask0	Expansion Bus Interrupt Mask Register 0	Read/Write
0xA800 0003	Ext Interrupt Mask1	Expansion Bus Interrupt Mask Register 1	Read/Write
0xA800 0004	Ext Interrupt Polarity Type0	Expansion Bus Interrupt Polarity Type Configuration Register 0	Write
0xA800 0005	Ext Interrupt Polarity Type1	Expansion Bus Interrupt Polarity Type Configuration Register 1	Write
0xA800 0006	Ext Interrupt Detection Type0	Expansion Bus Interrupt Detection Type Configuration Register 0	Write
0xA800 0007	Ext Interrupt Detection Type1	Expansion Bus Interrupt Detection Type Configuration Register 1	Write
0xA800 0008	Ext Bus Control	Expansion Bus Control Register	Read/Write
0xA800 0009	Ext I/F Control	CON11/CON19 Connection Control Register	Read/Write
0xA800 000A	RTC Control	Real-Time Clock Control Registers	Read/Write
0xA800 000B	Reserved		-
0xA800 000C	Reserved		-
0xA800 000D	Reserved		-
0xA800 000E	Reserved		-
0xA800 000F	CPLD Version	CPLD Version Register	Read

E.2. CPLD Registers

Details on the CPLD registers are covered below.

E.2.1. Ext Interrupt Status Register 0 (0xA800 0000)

Ext Interrupt Status Register 0 is used to observe and clear interrupts IRQ3, IRQ4, IRQ5, IRQ6 and IRQ7.

Table E.2. Ext Interrupt Status Register 0

	7	6	5	4	3	2	1	0
Read	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3			
Write								
RESET	0	0	0	0	0	-	-	-

Table E.3. Ext Interrupt Status Register 0 Description

Bits	Field	Description
7	IRQ7	Read Interrupt status prior to masking can be obtained. 1: Interrupt occurring 0: No interrupt Write 1: Interrupt clear (when interrupt set to EDGE)
6	IRQ6	
5	IRQ5	
4	IRQ4	
3	IRQ3	
2:0	Reserved	

E.2.2. Ext Interrupt Status Register 1 (0xA800 0001)

Ext Interrupt Status Register 1 is used to observe and clear interrupts IRQ9, IRQ10, IRQ11, IRQ12, IRQ14 and IRQ15.

Table E.4. Ext Interrupt Status Register 1

	7	6	5	4	3	2	1	0
Read	IRQ15	IRQ14		IRQ12	IRQ11	IRQ10	IRQ9	
Write								
RESET	0	0	-	0	0	0	0	-

Table E.5. Ext Interrupt Status Register 1 Description

Bits	Field	Description
7	IRQ15	Read Interrupt status prior to masking can be obtained. 1: Interrupt occurring 0: No interrupt Write 1: Interrupt clear (when interrupt set to EDGE)
6	IRQ14	
5	Reserved	
4	IRQ12	Read Interrupt status prior to masking can be obtained. 1: Interrupt occurring 0: No interrupt Write 1: Interrupt clear (when interrupt set to EDGE)
3	IRQ11	
2	IRQ10	
1	IRQ9	
0	Reserved	

E.2.3. Ext Interrupt Mask Register 0 (0xA800 0002)

Ext Interrupt Mask Register 0 is used to enable and disable interrupts IRQ3, IRQ4, IRQ5, IRQ6 and IRQ7.

Table E.6. Ext Interrupt Mask Register 0

	7	6	5	4	3	2	1	0
Read	MASK7	MASK6	MASK5	MASK4	MASK3			
Write								
RESET	0	0	0	0	0	-	-	-

Table E.7. Ext Interrupt Mask Register0 Description

Bits	Field	Description
7	MASK7	Used to configure interrupt enable and disable. 1: Enable 0: Disable (if interrupt is set to EDGE the interrupt state will be preserved)
6	MASK6	
5	MASK5	
4	MASK4	
3	MASK3	
2:0	Reserved	

E.2.4. Ext Interrupt Mask Register 1 (0xA800 0003)

Ext Interrupt Mask Register 1 is used to enable and disable interrupts IRQ9, IRQ10, IRQ11, IRQ12, IRQ14 and IRQ15.

Table E.8. Ext Interrupt Mask Register 1

	7	6	5	4	3	2	1	0
Read	MASK15	MASK14		MASK12	MASK11	MASK10	MASK9	
Write								
RESET	0	0	-	0	0	0	0	-

Table E.9. Ext Interrupt MASK Register1 Description

Bits	Field	Description
7	MASK15	Used to configure interrupt enable and disable. 1: Enable 0: Disable (if interrupt is set to EDGE the interrupt state will be preserved)
6	MASK14	
5	Reserved	
4	MASK12	Used to configure interrupt enable and disable. 1: Enable 0: Disable (if interrupt is set to EDGE the interrupt state will be preserved)
3	MASK11	
2	MASK10	
1	MASK9	
0	Reserved	

E.2.5. Ext Interrupt Polarity Type Register 0 (0xA800 0004)

Ext Interrupt Polarity Type Register 0 is used to configure the polarity of interrupts IRQ3, IRQ4, IRQ5, IRQ6 and IRQ7.

Table E.10. Ext Interrupt Polarity Type Register 0

	7	6	5	4	3	2	1	0
Read								
Write	POL7	POL6	POL5	POL4	POL3			
RESET	1	1	1	1	1	-	-	-

Table E.11. Ext Interrupt Polarity Type Register 0

Bits	Field	Description
7	POL7	Used to configure interrupt polarity. 1: RISING EDGE or LEVEL-HIGH 0: FALLING EDGE or LEVEL-LOW
6	POL6	
5	POL5	
4	POL4	
3	POL3	
2:0	Reserved	

E.2.6. Ext Interrupt Polarity Type Register 1 (0xA800 0005)

Ext Interrupt Polarity Type Register 1 is used to configure the polarity of interrupts IRQ9, IRQ10 and IRQ11. The polarity of IRQ12, IRQ14 and IRQ15 cannot be changed.

Table E.12. Ext Interrupt Polarity Type Register 1

	7	6	5	4	3	2	1	0
Read								
Write					POL11	POL10	POL9	
RESET	-	-	-	-	1	1	1	-

Table E.13. Ext Interrupt Polarity Type Register 1

Bits	Field	Description
7:4	Reserved	
3	POL11	Used to configure interrupt polarity. 1: RISING EDGE or LEVEL-HIGH 0: FALLING EDGE or LEVEL-LOW
2	POL10	
1	POL9	
0	Reserved	

E.2.7. Ext Interrupt Detection Type Register 0 (0xA800 0006)

Ext Interrupt Detection Type Register 0 is used to configure the detection type of interrupts IRQ3, IRQ4, IRQ5, IRQ6 and IRQ7.

Table E.14. Ext Interrupt Detection Select Register 0

	7	6	5	4	3	2	1	0
Read								
Write	DET7	DET6	DET5	DET4	DET3			
RESET	0	0	0	0	0	-	-	-

Table E.15. Ext Interrupt Detection Type Register 0

Bits	Field	Description
7	DET7	Used to configure interrupt detection type. 1: EDGE 0: LEVEL
6	DET6	
5	DET5	
4	DET4	
3	DET3	
2:0	Reserved	

E.2.8. Ext Interrupt Detection Type Register 1 (0xA800 0007)

Ext Interrupt Detection Type Register 1 is used to configure the detection type of interrupts IRQ9, IRQ10 and IRQ11. Interrupts IRQ12, IRQ14 and IRQ15 are fixed to LEVEL.

Table E.16. Ext Interrupt Detection Type Register 1

	7	6	5	4	3	2	1	0
Read								
Write					DET11	DET10	DET9	
RESET	-	-	-	-	0	0	0	-

Table E.17. Ext Interrupt Detection Type Register 1 Description

Bits	Field	Description
7:4	Reserved	
3	DET11	Used to configure interrupt detection type. 1: EDGE 0: LEVEL
2	DET10	
1	DET9	
0	Reserved	

E.2.9. Ext Bus Control Register (0xA800 0008)

Ext Bus Control Register is used to switch the expansion bus mode and perform resets.

Table E.18. Ext Bus Control Register

	7	6	5	4	3	2	1	0
Read					CLK_R	MODE (1)	MODE (0)	RST
Write								
RESET	-	-	-	-	0	0	0	1

Table E.19. Ext Bus Control Register Description

Bits	Field	Description
7:4	Reserved	
3	CLK_R	Changes clock phasing. 1: Invert 0: Output as is
2:1	MODE	11: Direct CPU Bus Mode (Synchronous), CS3 only 10: Reserved 01: Direct CPU Bus Mode (Asynchronous), CS3 and CS4 00: PC/104 Expansion Bus Compatibility Mode (Asynchronous)
0	RST	Used to configure output from RESET (pin 2 on J1) 1: High 0: Low

E.2.10. Ext I/F Control Register (0xA800 0009)

Ext I/F Control Register is used to configure the connection points of the KPP_COL0/GPIO3_1, KPP_COL1/GPIO3_2, KPP_COL2/GPIO3_3 and KPP_COL3/GPIO3_4 pins on i.MX257.

Table E.20. Ext I/F Control Register

	7	6	5	4	3	2	1	0
Read						EXT_IF_SEL (1)	EXT_IF_SEL (0)	EXT_IF_EN
Write								
RESET	-	-	-	-	-	0	0	0

Table E.21. Ext I/F Control Register Description

Bits	Field	Description
7:3	Reserved	
2:1	EXT_IF_SEL	Used to configure the connection points of the AUD5_TXD/UART4_RXD, AUD5_RXD/UART4_TXD, AUD5_TXC/UART4_RTS and AUD5_TXFS/UART4_CTS pins on i.MX257. 00: Connect to 3 (RXD4), 4 (RTS4), 5 (TXD4) and 6 (CTS4) on CON19 01: Reserved 10: Connect to 3 (RXD4) and 5 (TXD4) on CON19 and 46 (EXT_IO31) and 47 (EXT_IO32) on CON11 11: Connect to 44 (EXT_IO29), 45(EXT_IO30), 46(EXT_IO31) and 47(EXT_IO32) on CON11

Bits	Field	Description
0	EXT_IF_EN	Used to enable and disable the selector. 1: Enable 0: Disable

E.2.11. RTC Control Register (0xA800 000A)

RTC Control Register is used to control the data and clock lines of the real-time clock.

Table E.22. RTC Control Register

	7	6	5	4	3	2	1	0
Read							RTC_SCL	RTC_SDA
Write								
RESET	-	-	-	-	-	-	Z	Z

Table E.23. RTC Control Description

Bits	Field	Description
7:2	Reserved	
1	RTC_SCL	Used to control the SCL signal to the real-time clock. Write 1: Hi-Z 0: Low Read Reading can be performed after '1' has be written.
0	RTC_SDA	Used to control the SDA signal to the real-time clock. Write 1: Hi-Z 0: Low Read Reading can be performed after '1' has be written.

E.2.12. CPLD Version Register (0xA800 000F)

CPLD Version Register is the version register of the CPLD.

Table E.24. CPLD Version Register

	7	6	5	4	3	2	1	0
Read	CPLD_VER							
Write								
RESET	CPLD Version Number							

Table E.25. CPLD Version Register Description

Bits	Field	Description
7:0	CPLD_VER	The version number of the CPLD.

Revision History

Revision	Date	Description
1.0.0	03/12/2010	• Initial Release
1.1.0	04/30/2010	• Added explanation of Armadillo-400 Series to Chapter 1, Preface • Added Section 1.3, “Icons” • Added Section 2.5, “Electromagnetic Interference” • Added "Armadillo-420" to Table 3.1, “Armadillo-400 Series Board Specifications” • Made corrections to Figure 3.1, “Armadillo-420/440 Block Diagram” • Added "Armadillo-420" to Table 4.1, “Physical Memory Map - Armadillo-420/440” • Added Section 5.1.1, “Armadillo-420 Interface Layout” • Added precaution notes to Section 5.3.1, “CON1 (SD Interface) - Armadillo-420/440” and Section 6.3.1, “CON1, CON23, CON25 (SD Interface) - Armadillo-460” • Added Section 8.1, “Armadillo-420 Board Outline Diagrams” • Added Section 9.2, “Armadillo-400 Series RTC Option Module (Product ID: OP-A400RTCMOD-00)” • Added Appendix A, Armadillo-400 Series JTAG Conversion Cable (OP-JC8P25-00)
1.2.0	06/08/2010	• Added explanation of GPIO control of supply power to Section 5.3.1, “CON1 (SD Interface) - Armadillo-420/440” and Section 6.3.1, “CON1, CON23, CON25 (SD Interface) - Armadillo-460” • Added Figure 5.4, “EXT_RESET* Timing Chart - Armadillo-420/440” • Added Figure 5.5, “EXT_RESET* Circuit Make-up - Armadillo-420/440” • Added Table 5.16, “CON9 Signal Multiplex - Armadillo-420/440” • Added Table 5.19, “CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-420/440” • Added Table 5.23, “CON14 Signal Multiplex - Armadillo-420/440” • Added explanation of JTAG Conversion Cable option to Section 5.3.7, “CON10 (i.MX257 JTAG Interface) - Armadillo-420/440” • Added Section 3.2.2, “Power Circuit Make-up - Armadillo-420/440” • Added Figure 7.2, “Keypad Signals Reference Circuit” • Added Figure 7.3, “CAN Signals Reference Circuit” • Added annotation to Table 9.7, “RTC Option Module (Product ID: OP-A400RTCMOD-00) Specifications” • Added Appendix B, Initial Configuration State of Expansion Interfaces
1.3.0	08/20/2010	• Added Appendix C, Connector Information • Added Table 5.3, “Input/Output Interface Rated Absolute Maximum - Armadillo-420/440” • Added product number and write cycle information of flash memory to Table 3.1, “Armadillo-400 Series Board Specifications” • Added information on internal circuit current consumption to Figure 3.2, “Armadillo-420/440 Power Circuit Make-up Diagram” • Changed Figure A.3, “JTAG Conversion Cable Reference Circuit” to a more readable diagram • Changed Figure 5.5, “EXT_RESET* Circuit Make-up - Armadillo-420/440” to a more readable diagram • Changed Figure 7.2, “Keypad Signals Reference Circuit” to a more readable diagram • Changed Figure 7.3, “CAN Signals Reference Circuit” to a more readable diagram

		• Added Section 9.2.4, “Assembly” • Added Chapter 10, Case • Added explanation to Section 9.2.1, “Board Overview”
1.4.0	12/25/2010	• Corrected Table 5.16, “CON9 Signal Multiplex - Armadillo-420/440” • Corrected Table 5.19, “CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-420/440” • Corrected Table 5.23, “CON14 Signal Multiplex - Armadillo-420/440” • Added SIM signals to Table 5.16, “CON9 Signal Multiplex - Armadillo-420/440” and Table 5.19, “CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-420/440” • Added CAN signals to Table 5.19, “CON11 Signal Multiplexing (pins 1 - 38) - Armadillo-420/440” • Added a precaution note about reserved regions to Section 2.3, “Software Usage Precautions” • Chapter 2, Precautions was completely rewritten • Added "Product Revision B" content to Section 9.1, “Armadillo-400 Series LCD Expansion Board” • Added Section 9.3, “Armadillo-400 Series RTC Option Module (Product ID: OP-A400RTCMOD-01)” • Added Section 9.4, “Armadillo-400 Series WLAN Option Module (AWL12 Compatible) (Product ID: OP-A400-AWLMOD-00)” • Added Section 10.2, “Plastic Case (Product ID: OP-CASE400-MET-00)” to Chapter 10, Case • Corrected product name usage inconsistencies
1.4.1	03/25/2011	• Updated company address • Corrected various errata and usage inconsistencies
1.5.0	07/13/2011	• Added information on Armadillo-460 • Added more detailed information to Table 3.1, “Armadillo-400 Series Board Specifications” • Corrected various errata and usage inconsistencies
1.6.0	08/26/2011	• Altered section layout of Section 3.1, “Board Overview” • Altered section layout of Section 5.1, “Interface Layout - Armadillo-420/440” • Added Section 6.1, “Interface Layout - Armadillo-460” and adjusted section numbering • Changed title of Section 7.1, “Reference Circuits” and added Section 7.2, “Towards Productization” • Added mountable connectors to Table C.2, “Connector Product Numbers List” • Corrected tah to 33ns in Table 6.47, “PC/104 Expansion Bus Compatibility Mode Bus Access Timing” • Corrected signal state of pin 27 after reset to "undefined" in Table B.1, “Signal State of Expansion Interfaces (After i.MX257 Reset)”
1.6.1	10/21/2011	• Made format corrections to Figure 3.1, “Armadillo-420/440 Block Diagram” • Made format corrections to Figure 3.4, “Armadillo-460 Block Diagram” • Updated VCCI Class A information in Section 2.5, “Electromagnetic Interference” • Corrected various errata and usage inconsistencies • Updated web site name
1.7.0	12/21/2011	• Made format corrections to Figure 3.1, “Armadillo-420/440 Block Diagram” • Made corrections to Figure 3.4, “Armadillo-460 Block Diagram”

		• Made corrections to Figure 3.2, “Armadillo-420/440 Power Circuit Make-up Diagram” • Made corrections to Figure 6.3, “CON11/CON19 Connection Selector - Armadillo-460” • Updated VCCI Class A information in Section 2.5, “Electromagnetic Interference” • Added Section 9.5, “Armadillo-400 Series WLAN Option Module (AWL13 Compatible) (Product ID: OP-A400-AWLMOD-10)” • Updated web site name • Corrected various errata and usage inconsistencies

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