

# TCA9555 低電圧、16 ビット I<sup>2</sup>C および SMBus I/O エクスパンダ、 割り込み出力、構成レジスタ付き

## 1 特長

- 低いスタンバイ時消費電流：3.5 $\mu$ A 以下
- I<sup>2</sup>Cからパラレル・ポートへのエクスパンダ
- オープン・ドレインのアクティブLOW割り込み出力
- 5V対応のI/Oポート
- ほとんどのマイクロコントローラと互換
- 400kHzのFast I<sup>2</sup>Cバス
- 3本のアドレス・ピンでスレーブ・アドレスを設定可能
- 極性反転レジスタ
- 大電流の駆動能力を持つラッチ付き出力により、LEDを直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22を超えるESD保護
  - 2000V、人体モデル(A114-A)
  - 1000V、荷電デバイス・モデル(C101)

## 2 アプリケーション

- サーバー
- ルーター(テレコム・スイッチング機器)
- パーソナル・コンピュータ
- パーソナル・エレクトロニクス
- 産業オートメーション機器
- GPIOが制限されたプロセッサを使用する製品

## 3 概要

この 2 線式双方向バス (I<sup>2</sup>C) 用 16 ビット I/O エクスパンダは、1.65V~5.5V の V<sub>CC</sub> で動作するように設計されています。I<sup>2</sup>C インターフェイスにより、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張に使用できます。

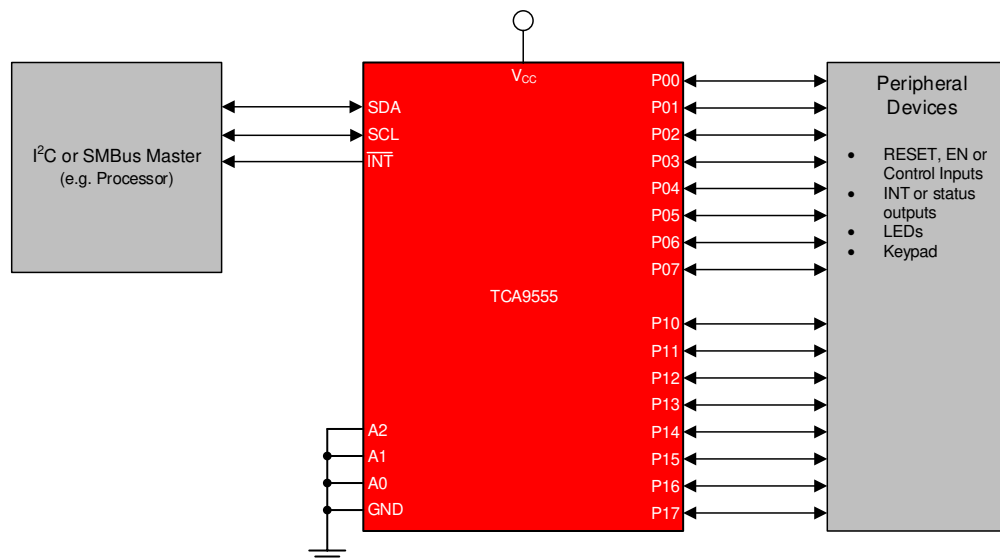
TCA9555 は、構成 (入力/出力選択)、入力ポート、出力ポート、極性反転 (アクティブ HIGH またはアクティブ LOW 動作) 用の 8 ビット・レジスタをそれぞれ 2 個ずつ搭載しています。電源オン時に、I/Oは入力として構成されます。システム・マスタは、I/O構成ビットに書き込むことで、I/Oを入力または出力としてイネーブルできます。それぞれの入力または出力のデータは、対応する入力または出力レジスタに保持されます。入力ポート・レジスタの極性は、極性反転レジスタで反転できます。

### 製品情報(1)

型番	パッケージ	本体サイズ(公称)
TCA9555	TSSOP (24) PW	7.80mm x 4.40mm
	SSOP (24) DB	8.20mmx5.30mm
	WQFN (24) RTW	4.00mmx4.00mm
	VQFN (24) RGE	4.00mmx4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 概略回路図



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (July 2016) から Revision E に変更	Page
• 「製品情報」表を変更	1
• Changed the Pin Configuration images	4

Revision C (June 2016) から Revision D に変更	Page
• 「製品情報」表に DB パッケージを追加	1

Revision A (July 2009) から Revision B に変更	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1

Revision B (July 2015) から Revision C に変更	Page
• 「製品情報」表に RGE パッケージを追加	1
• Changed V <sub>IH</sub> for I <sup>2</sup> C pins limited to V <sub>CC</sub> , with note allowing higher voltage	5
• Added I <sub>OL</sub> for different T <sub>j</sub>	5
• Removed ΔI <sub>CC</sub> spec from the <i>Electrical Characteristics</i> table, added ΔI <sub>CC</sub> typical characteristics graph	6
• Changed I <sub>CC</sub> standby into different input states	7
• Changed C <sub>io</sub> maximum	7
• Changed Typical characteristic plots with updated data	9
• POR requirements, bounded lowest voltage allowed during glitch	30

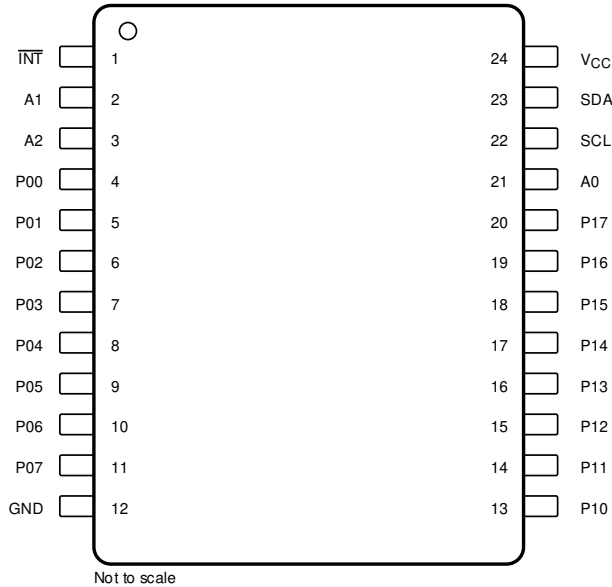
## 5 概要 (続き)

TCA9555 は、I/O プルアップ抵抗を内蔵していることを除き TCA9535 と同じです。この I/O プルアップ抵抗は、I/O が入力として構成されている場合または駆動されていない場合に、I/O をデフォルトの HIGH にプルアップします。

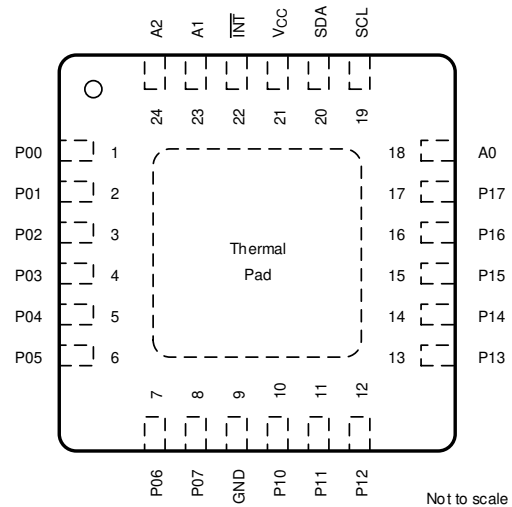
3 本のハードウェア・ピン (A0、A1、A2) は、I<sup>2</sup>C アドレスのプログラムに使用され、最大 8 つの TCA9555 デバイスが同じ I<sup>2</sup>C バスまたは SMBus を共有できます。TCA9555 の固定 I<sup>2</sup>C アドレスは、PCF8575、PCF8575C、PCF8574 と同一であるため、これらのデバイスは最大 8 つまで任意の組み合わせで同じ I<sup>2</sup>C バスまたは SMBus を共有できます。

## 6 Pin Configuration and Functions

**DB, PW Package  
24-Pin TSSOP  
Top View**



**RTW, RGE Package  
24-Pin WQFN, VQFN with Exposed Thermal Pad  
Top View**



The exposed thermal pad, if used, must be connected as a secondary ground or left electrically open.

### Pin Functions

NAME	PIN NO.		TYPE	DESCRIPTION
	DB, PW	RTW, RGE		
A0	21	18	Input	Address input 0. Connect directly to V <sub>CC</sub> or ground
A1	2	23	Input	Address input 1. Connect directly to V <sub>CC</sub> or ground
A2	3	24	Input	Address input 2. Connect directly to V <sub>CC</sub> or ground
GND	12	9	GND	Ground
INT	1	22	Output	Interrupt output. Connect to V <sub>CC</sub> through a pull-up resistor
P00	4	1	I/O	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
P01	5	2	I/O	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
P02	6	3	I/O	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
P03	7	4	I/O	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
P04	8	5	I/O	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
P05	9	6	I/O	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
P06	10	7	I/O	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
P07	11	8	I/O	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input
P10	13	10	I/O	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input
P11	14	11	I/O	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
P12	15	12	I/O	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
P13	16	13	I/O	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
P14	17	14	I/O	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
P15	18	15	I/O	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
P16	19	16	I/O	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
P17	20	17	I/O	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
SCL	22	19	Input	Serial clock bus. Connect to V <sub>CC</sub> through a pull-up resistor
SDA	23	20	Input	Serial data bus. Connect to V <sub>CC</sub> through a pull-up resistor
V <sub>CC</sub>	24	21	Supply	Supply voltage

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	6	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	6	V
V <sub>O</sub>	Output voltage <sup>(2)</sup>	-0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-20	mA
I <sub>I<sub>OK</sub></sub>	Input-output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>	50	mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-50	mA
I <sub>CC</sub>	Continuous current through GND		-250	mA
	Continuous current through V <sub>CC</sub>		160	
T <sub>j(MAX)</sub>	Maximum junction temperature		100	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	V <sub>CC</sub> <sup>(1)</sup>
		A2–A0, P07–P00, P17–P10	0.7 × V <sub>CC</sub>	5.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub>
		A2–A0, P07–P00, P17–P10	-0.5	0.3 × V <sub>CC</sub>
I <sub>OH</sub>	High-level output current	P07–P00, P17–P10	-10	mA
I <sub>OL</sub>	Low-level output current <sup>(2)</sup>	P07–P00, P17–P10	T <sub>j</sub> ≤ 65°C	25
			T <sub>j</sub> ≤ 85°C	18
			T <sub>j</sub> ≤ 100°C	11
I <sub>OL</sub>	Low-level output current <sup>(2)</sup>	$\overline{\text{INT}}$ , SDA	T <sub>j</sub> ≤ 85°C	6
			T <sub>j</sub> ≤ 100°C	3.5
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) For voltages applied above V<sub>CC</sub>, an increase in I<sub>CC</sub> results.
- (2) The values shown apply to specific junction temperatures, which depend on the R<sub>θJA</sub> of the package used. See the [Calculating Junction Temperature and Power Dissipation](#) section on how to calculate the junction temperature.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9555				UNIT
		PW (TSSOP)	DB (SSOP)	RTW (WQFN)	RGE (VQFN)	
		24 PINS	24 PINS	24 PINS	24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	108.8	92.9	43.6	48.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	54	53.5	46.2	58.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	62.8	50.4	22.1	27.1	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	11.1	21.9	1.5	3.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.3	50.1	22.2	27.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.7	15.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	1.65 V to 5.5 V	-1.2			V
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V		1.2	1.5	V
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	0.75	1		V
V <sub>OH</sub>	P-port high-level output voltage <sup>(2)</sup>	I <sub>OH</sub> = -8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.75 V	4.1			
		I <sub>OH</sub> = -10 mA	1.65 V	1			
			2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I <sub>OL</sub>	Low-level output current	SDA	V <sub>OL</sub> = 0.4 V	1.65 V to 5.5 V	3		mA
		P port <sup>(3)</sup>	V <sub>OL</sub> = 0.5 V	1.65 V to 5.5 V	8		mA
			V <sub>OL</sub> = 0.7 V	1.65 V to 5.5 V	10		mA
		$\overline{\text{INT}}$	V <sub>OL</sub> = 0.4 V	1.65 V to 5.5 V	3		mA
I <sub>I</sub>	Input leakage current	SCL, SDA Input leakage	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		±1	μA
		A2–A0 Input leakage	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		±1	μA
I <sub>IH</sub>	Input high leakage current	P port	V <sub>I</sub> = V <sub>CC</sub>	1.65 V to 5.5 V		1	μA
I <sub>IL</sub>	Input low leakage current	P port	V <sub>I</sub> = GND	1.65 V to 5.5 V		-100	μA

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.

(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

## Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
I <sub>CC</sub>	Quiescent current	Operating mode	I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 400 kHz, t <sub>r</sub> = 3 ns, No load	5.5 V		22	40	μA	
				3.6 V		11	30		
				2.7 V		8	19		
				1.95 V		5	11		
	Quiescent current	Standby mode	Low inputs	V <sub>I</sub> = GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz, No load	5.5 V		1.1	1.5	mA
					3.6 V		0.7	1.3	
					2.7 V		0.5	1	
					1.95 V		0.3	0.9	
		Standby mode	High inputs	V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz, No load	5.5 V		2.5	3.5	μA
					3.6 V		1	1.8	
					2.7 V		0.7	1.6	
					1.95 V		0.5	1	
C <sub>I</sub>	Input capacitance	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		3	8	pF	
C <sub>io</sub>	Input-output pin capacitance	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		3	9.5	pF	
		P port				3.7	9.5		

## 7.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 19)

				MIN	MAX	UNIT
<b>I<sup>2</sup>C BUS—STANDARD MODE</b>						
f <sub>scl</sub>	I <sup>2</sup> C clock frequency			0	100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time			4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time			4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time				50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time			250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time			0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time				1000	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time				300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time		10-pF to 400-pF bus		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start			4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup			4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold			4		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup			4		μs
t <sub>vd(data)</sub>	Valid data time		SCL low to SDA output valid		3.45	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition		ACK signal from SCL low to SDA (out) low		3.45	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load				400	pF
<b>I<sup>2</sup>C BUS—FAST MODE</b>						
f <sub>scl</sub>	I <sup>2</sup> C clock frequency			0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time			0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time			1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time				50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time			100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time			0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time			20	300	ns

## I<sup>2</sup>C Interface Timing Requirements (continued)

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 19](#))

		MIN	MAX	UNIT
t <sub>icf</sub>	I <sup>2</sup> C input fall time	20 × (V <sub>CC</sub> / 5.5 V)	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus	20 × (V <sub>CC</sub> / 5.5 V)	300
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	0.6		μs
t <sub>vd(data)</sub>	Valid data time	SCL low to SDA output valid	0.9	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.9	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

## 7.7 Switching Characteristics

 over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see [Figure 20](#) and [Figure 21](#))

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>iv</sub>	Interrupt valid time	P port	$\overline{\text{INT}}$		4	μs
t <sub>ir</sub>	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	μs
t <sub>pv</sub>	Output data valid; For V <sub>CC</sub> = 2.3 V–5.5 V	SCL	P port		200	ns
	Output data valid; For V <sub>CC</sub> = 1.65 V–2.3 V				300	ns
t <sub>ps</sub>	Input data setup time	P port	SCL	150		ns
t <sub>ph</sub>	Input data hold time	P port	SCL	1		μs



## 7.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

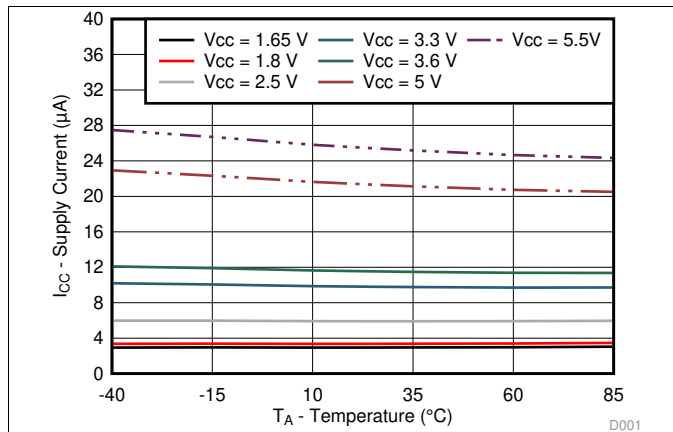


Figure 1. Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )

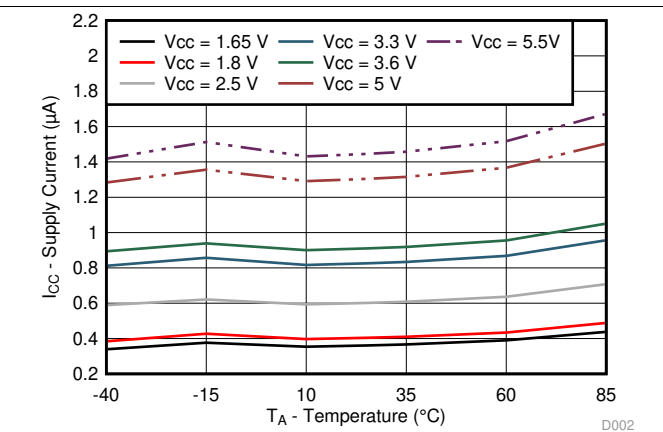


Figure 2. Standby Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )

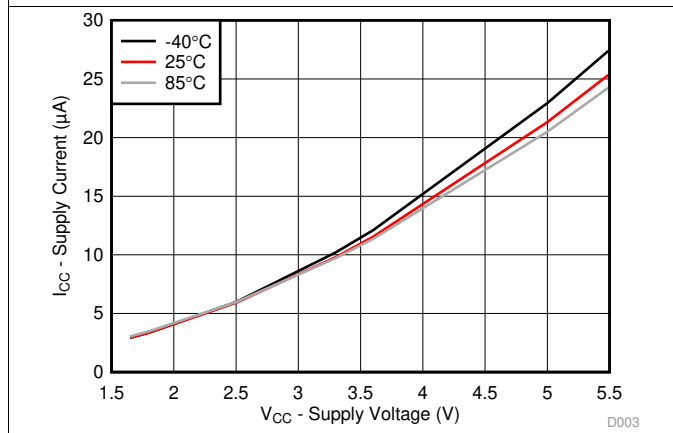


Figure 3. Supply Current vs Supply Voltage for Different Temperature ( $T_A$ )

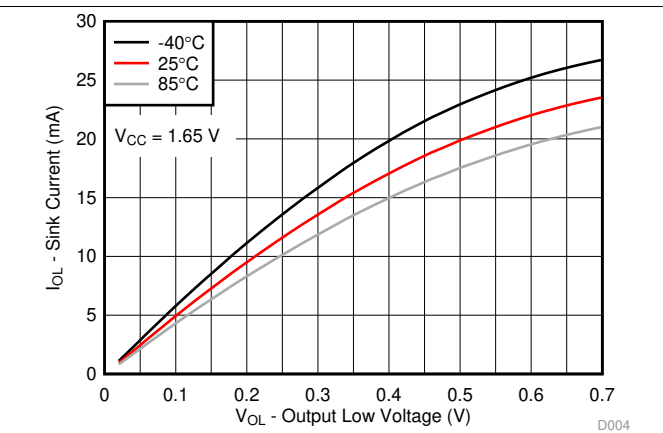


Figure 4. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$

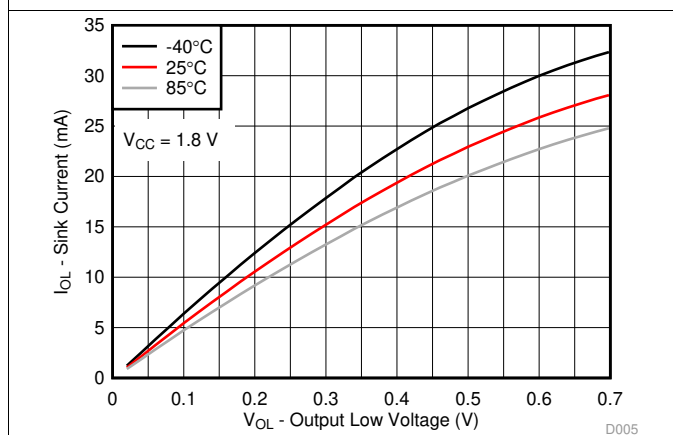


Figure 5. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$

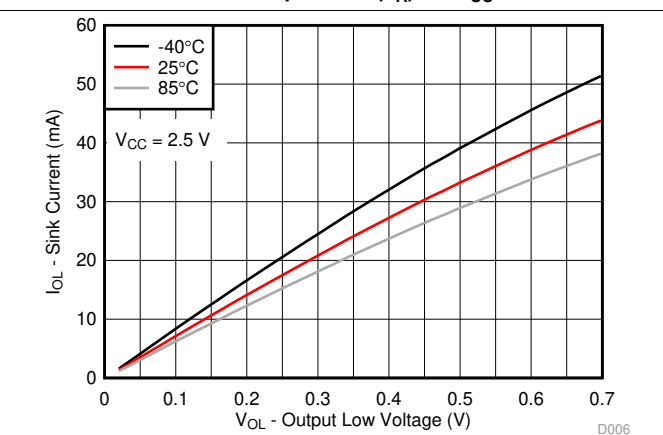


Figure 6. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 2.5\text{ V}$

### Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

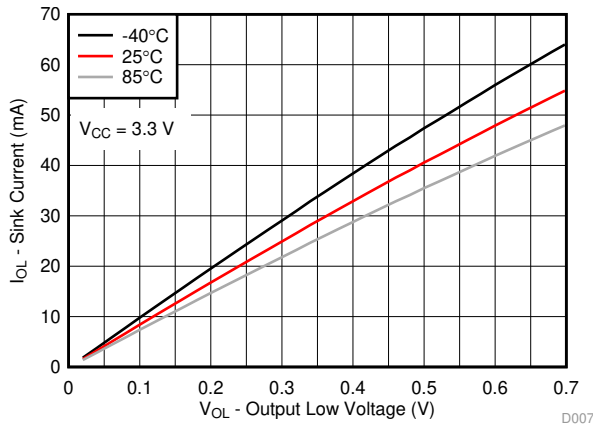


Figure 7. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 3.3\text{ V}$

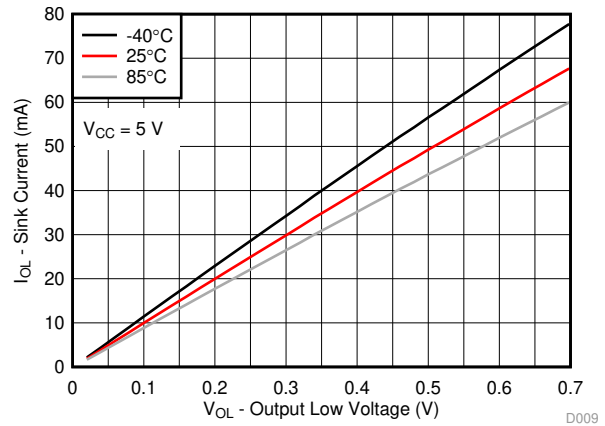


Figure 8. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5\text{ V}$

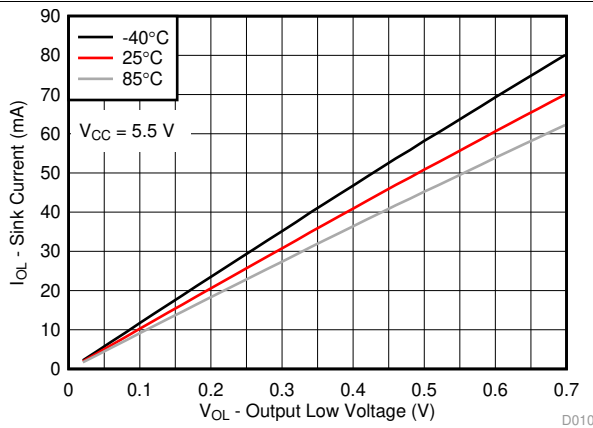


Figure 9. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5.5\text{ V}$

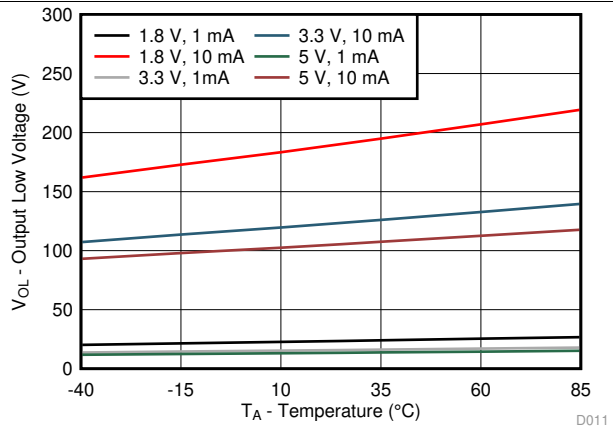


Figure 10. I/O Low Voltage vs Temperature for Different  $V_{CC}$  and  $I_{OL}$

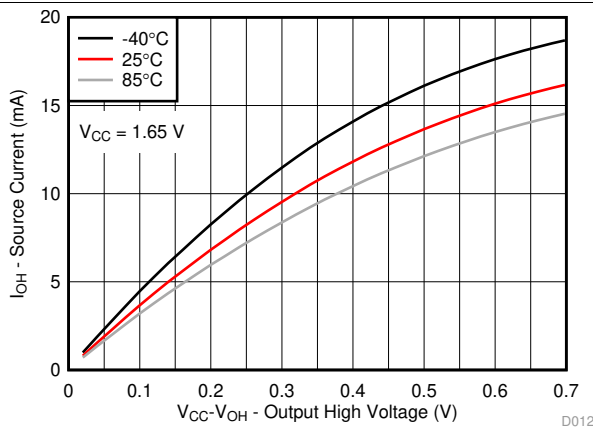


Figure 11. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$

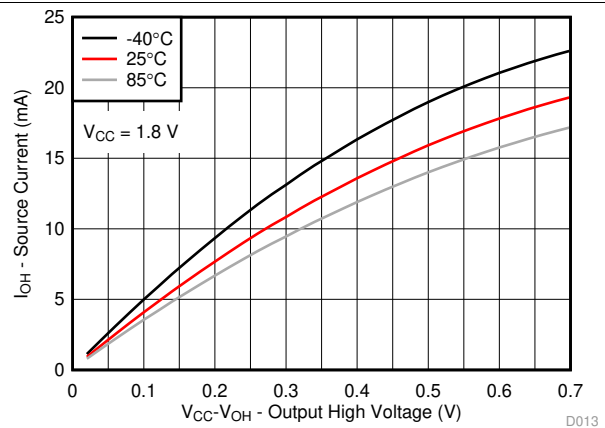


Figure 12. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$

Typical Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise noted)

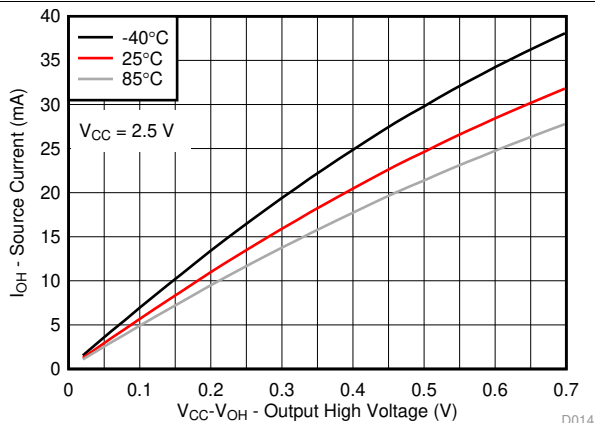


Figure 13. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 2.5 V

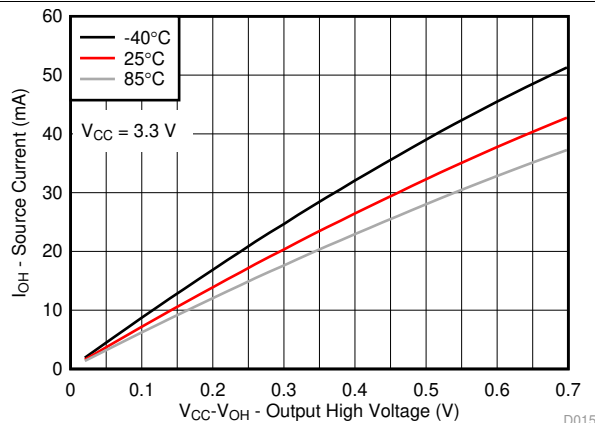


Figure 14. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 3.3 V

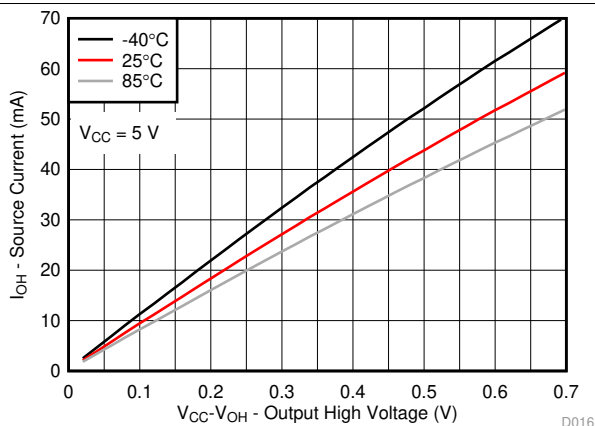


Figure 15. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 5 V

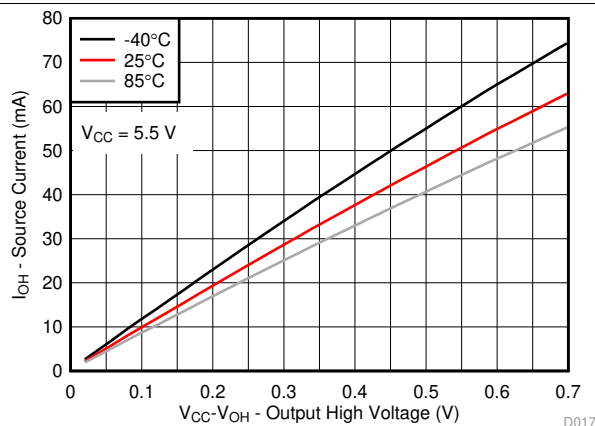


Figure 16. I/O Source Current vs Output High Voltage for Different Temperature (T<sub>A</sub>) for V<sub>CC</sub> = 5.5 V

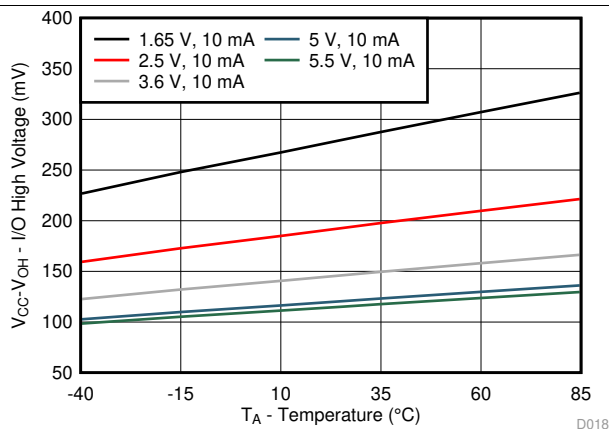


Figure 17. V<sub>CC</sub> – V<sub>OH</sub> Voltage vs Temperature for Different V<sub>CC</sub>

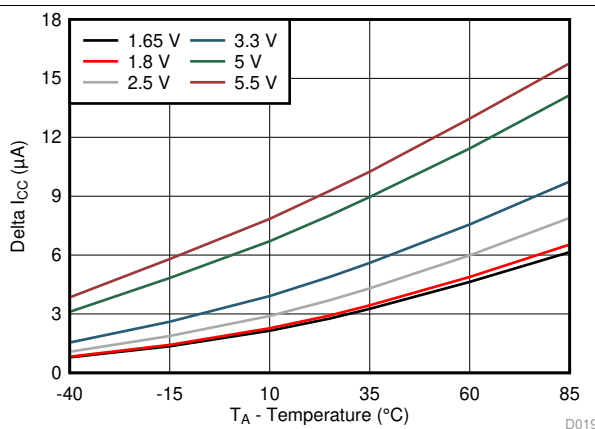
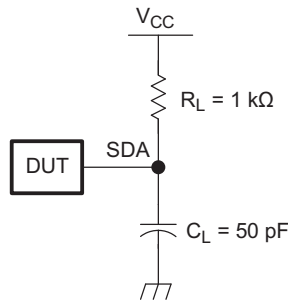
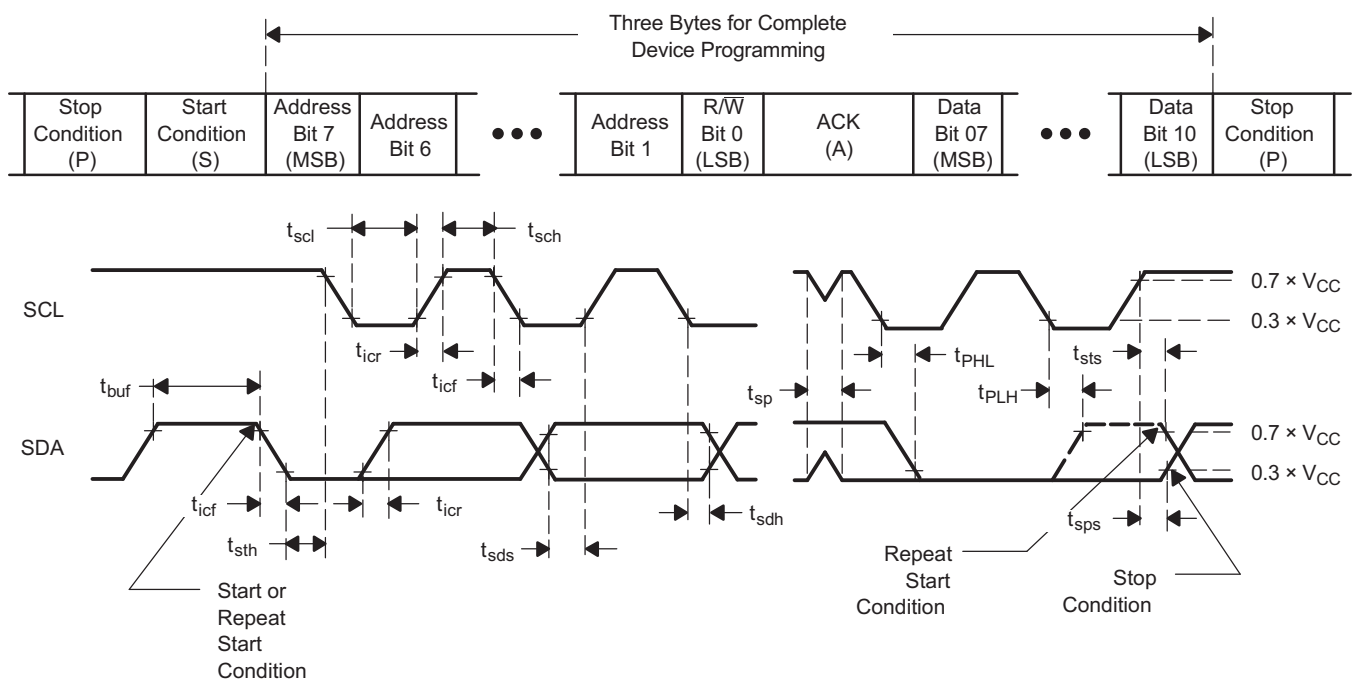


Figure 18. Δ I<sub>CC</sub> vs Temperature for Different V<sub>CC</sub> (V<sub>I</sub> = V<sub>CC</sub> – 0.6 V)

## 8 Parameter Measurement Information



SDA LOAD CONFIGURATION



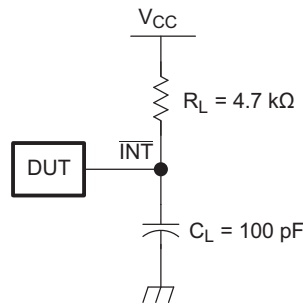
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

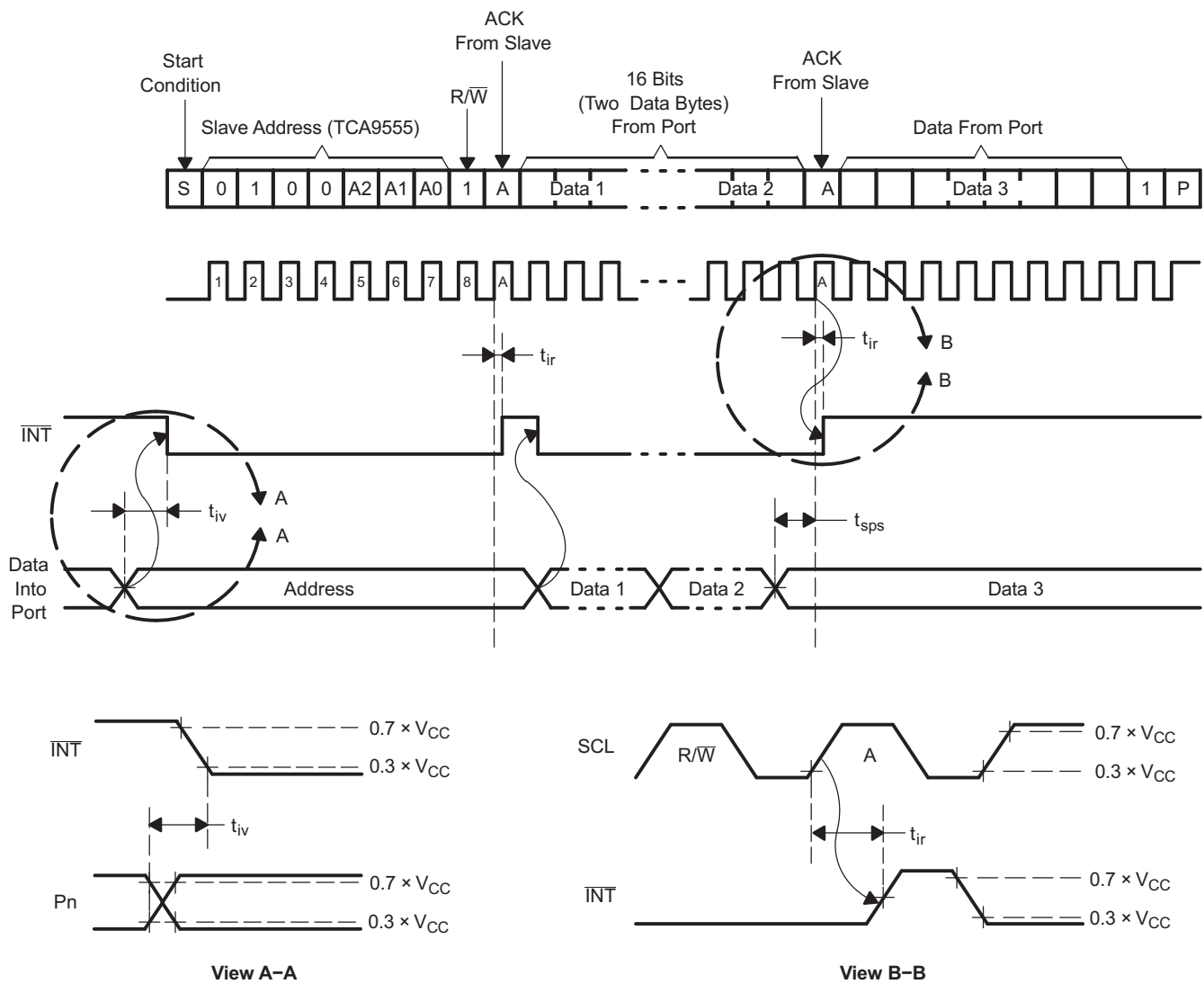
- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 19. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

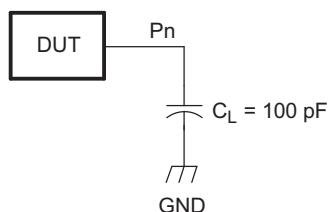
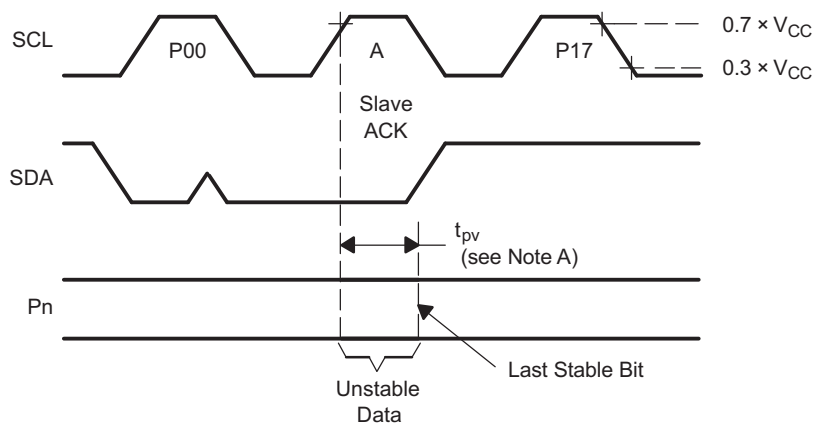
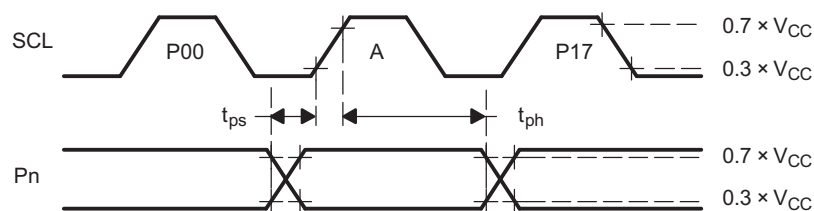


INTERRUPT LOAD CONFIGURATION



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 20. Interrupt Load Circuit and Voltage Waveforms

**Parameter Measurement Information (continued)**

**P-PORT LOAD CONFIGURATION**

**WRITE MODE ( $R/\bar{W} = 0$ )**

**READ MODE ( $R/\bar{W} = 1$ )**

- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O (Pn) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 21. P-Port Load Circuit and Voltage Waveforms**

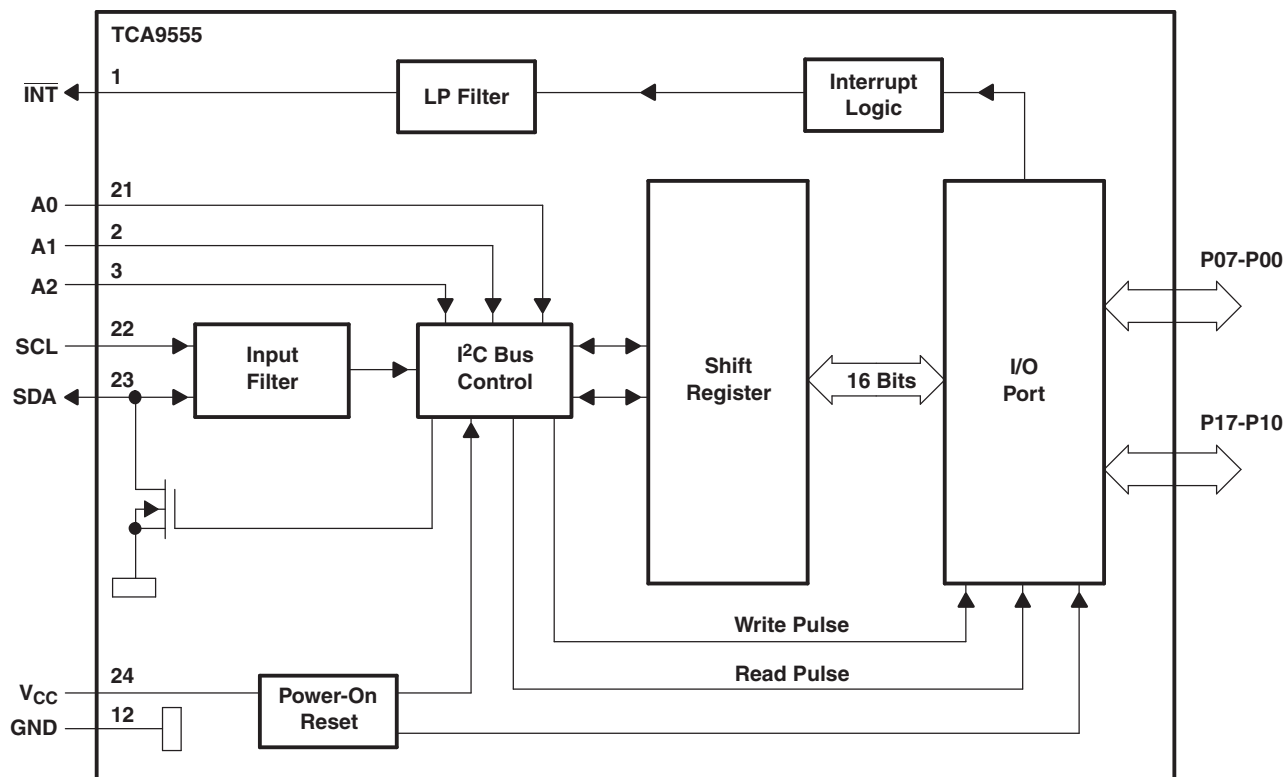
## 9 Detailed Description

### 9.1 Overview

The TCA9555 is a 16-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface.

One of the features of the TCA9555, is that the  $\overline{\text{INT}}$  output can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the TCA9555 can remain a simple slave device.

### 9.2 Functional Block Diagram



Pin numbers shown are for the PW package.

All I/Os are set to inputs at reset.

Figure 22. Logic Diagram (Positive Logic)

### 9.3 Feature Description

#### 9.3.1 5-V Tolerant I/O Ports

The TCA9555 features I/O ports which are tolerant of up to 5 V. This allows the TCA9555 to be connected to a large array of devices. To minimize ICC, any inputs must be sure that the input voltage stays within V<sub>IH</sub> and V<sub>IL</sub> of the device as described in the [Electrical Characteristics](#) table.

## Feature Description (continued)

### 9.3.2 Hardware Address Pins

The TCA9555 features 3 hardware address pins (A0, A1, and A2) to allow the user to program the device's I<sup>2</sup>C address by pulling each pin to either V<sub>CC</sub> or GND to signify the bit value in the address. This allows up to 8 TCA9555 to be on the same bus without address conflicts. See the [Functional Block Diagram](#) to see the 3 pins. The voltage on the pins must not change while the device is powered up in order to prevent possible I<sup>2</sup>C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to V<sub>CC</sub> or GND and cannot be left floating.

### 9.3.3 Interrupt ( $\overline{\text{INT}}$ ) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time  $t_{iv}$ , the signal INT is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the  $\overline{\text{INT}}$  is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as INT.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{\text{INT}}$  has an open-drain structure and requires a pull-up resistor to V<sub>CC</sub> (typically 10 k $\Omega$  in value).

## 9.4 Device Functional Modes

### 9.4.1 Power-On Reset (POR)

When power (from 0 V) is applied to V<sub>CC</sub>, an internal power-on reset circuit holds the TCA9555 in a reset condition until V<sub>CC</sub> has reached V<sub>POR</sub>. At that time, the reset condition is released, and the TCA9555 registers and I<sup>2</sup>C-SMBus state machine initialize to their default states. After that, V<sub>CC</sub> must be lowered to below V<sub>PORF</sub> and back up to the operating voltage for a power-reset cycle.

### 9.4.2 Powered-Up

When power has been applied to V<sub>CC</sub> above V<sub>POR</sub>, and the POR has taken place, the device is in a functioning mode. In this state, the device is ready to accept any incoming I<sup>2</sup>C requests and is monitoring for changes on the input ports.

## 9.5 Programming

### 9.5.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V<sub>CC</sub> to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V<sub>CC</sub> or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation. [Figure 23](#) shows the simplified schematic of P-Port I/Os.



## Programming (continued)

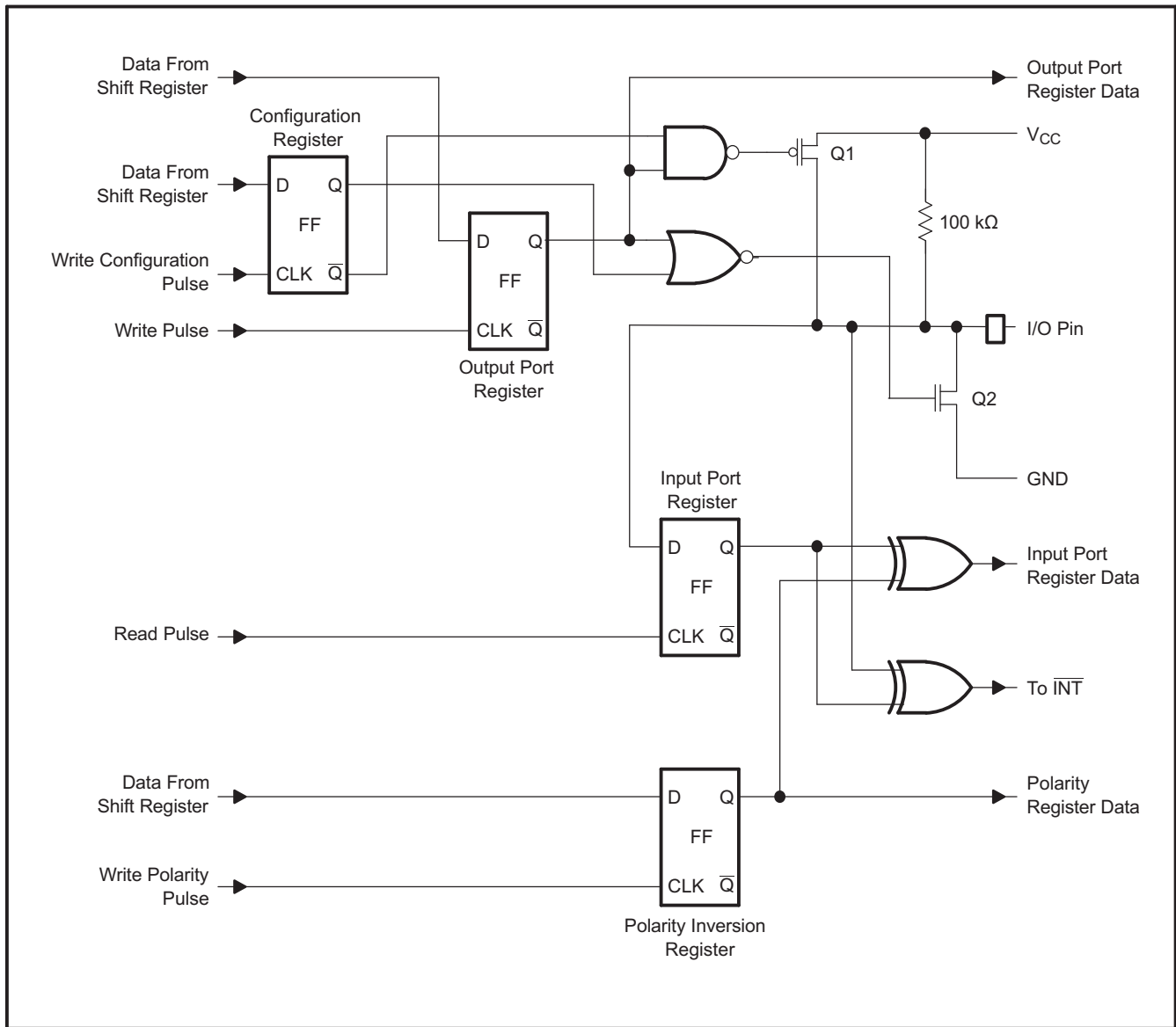


Figure 23. Simplified Schematic of P-Port I/Os

### 9.5.2 I<sup>2</sup>C Interface

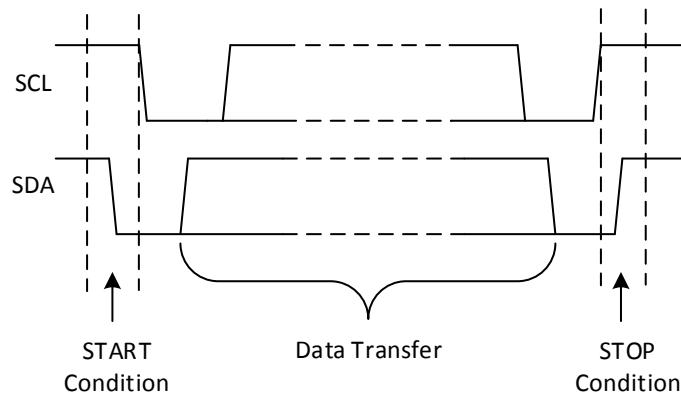
The TCA9555 has a standard bidirectional I<sup>2</sup>C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I<sup>2</sup>C bus has a specific device address to differentiate between other slave devices that are on the same I<sup>2</sup>C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see the *Understanding the I2C Bus* application report, [SLVA704](#).

The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V<sub>CC</sub> through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. For further details, refer to *I<sup>2</sup>C Pull-up Resistor Calculation* application report, [SLVA689](#). Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

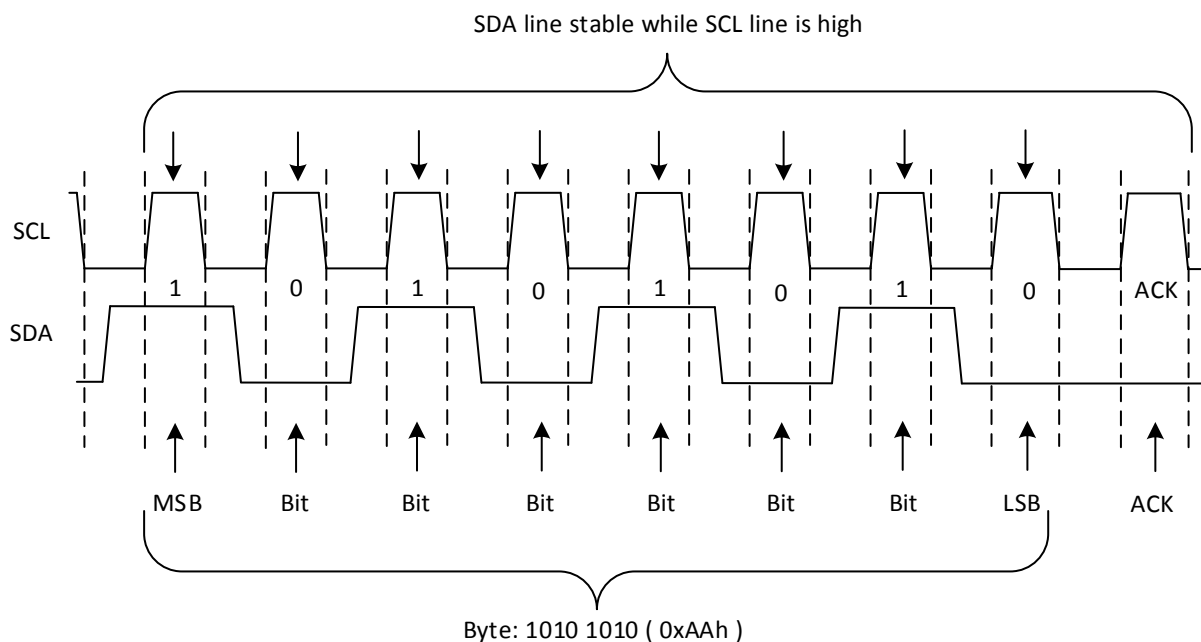
### Programming (continued)

Figure 24 and Figure 25 show the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
  - Master-transmitter sends a START condition and addresses the slave-receiver.
  - Master-transmitter sends data to slave-receiver.
  - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
  - Master-receiver sends a START condition and addresses the slave-transmitter.
  - Master-receiver sends the requested register to read to slave-transmitter.
  - Master-receiver receives data from the slave-transmitter.
  - Master-receiver terminates the transfer with a STOP condition.



**Figure 24. Definition of Start and Stop Conditions**



**Figure 25. Bit Transfer**

## Programming (continued)

Table 1 shows the interface definition.

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	L	L	A2	A1	A0	R/W
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

### 9.5.2.1 Bus Transactions

Data is exchanged between the master and the TCA9555 through write and read commands, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

#### 9.5.2.1.1 Writes

To write on the I<sup>2</sup>C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/W bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See the [Control Register and Command Byte](#) section to see list of the TCA9555's internal registers and a description of each one.

Figure 26 to Figure 28 show examples of writing a single byte to a slave register.

- Master controls SDA line
- Slave controls SDA line

#### Write to one register in a device

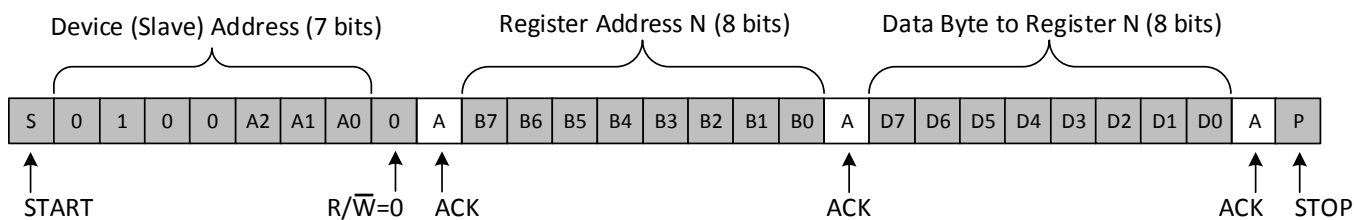
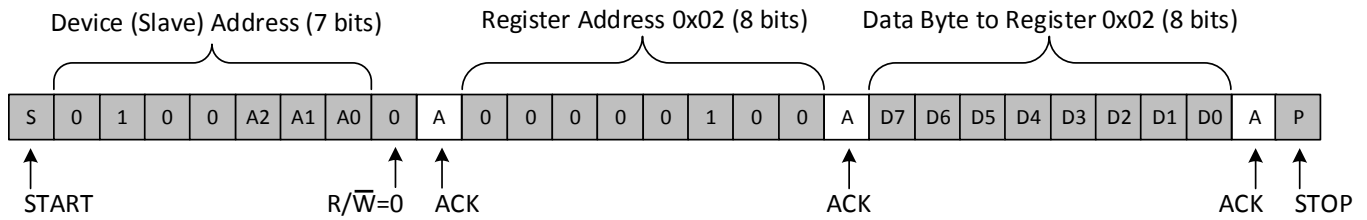


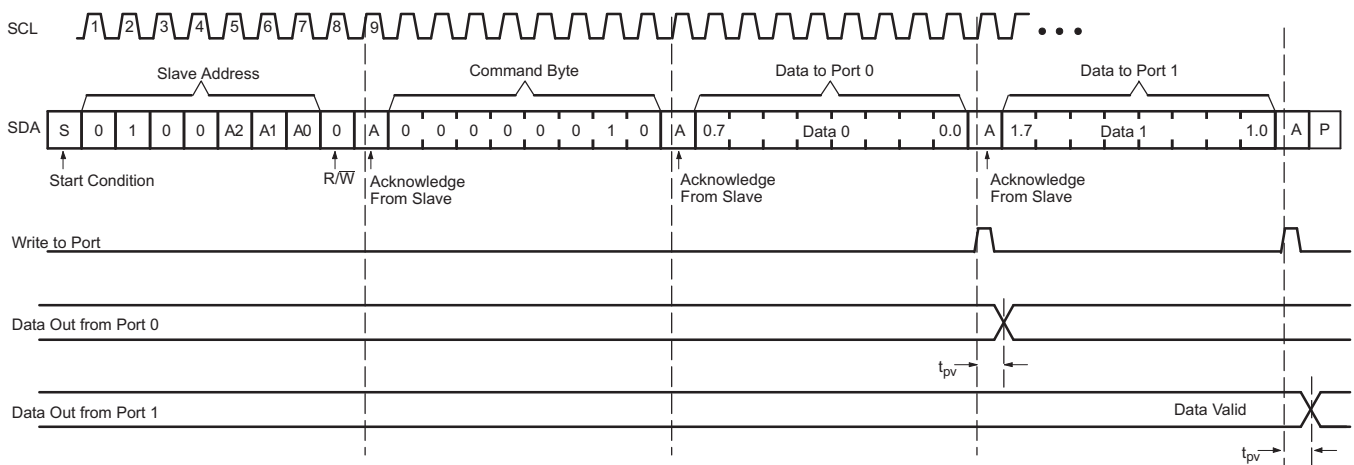
Figure 26. Write to Register

**Programming (continued)**

- Master controls SDA line
- Slave controls SDA line



**Figure 27. Write to the Polarity Inversion Register**



**Figure 28. Write to Output Port Registers**

## Programming (continued)

### 9.5.2.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/W bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

See the [Control Register and Command Byte](#) section to see list of the TCA9555's internal registers and a description of each one.

Figure 29 to Figure 31 show examples of reading a single byte from a slave register.

- Master controls SDA line
- Slave controls SDA line

#### Read from one register in a device

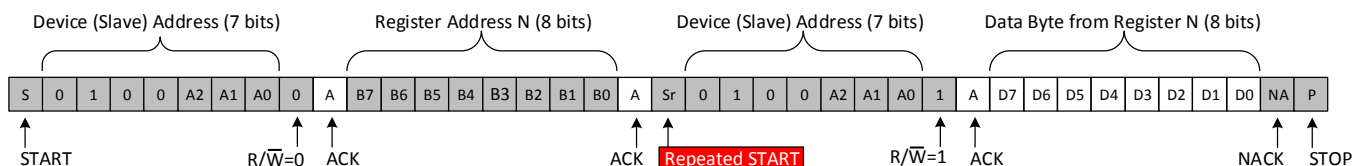
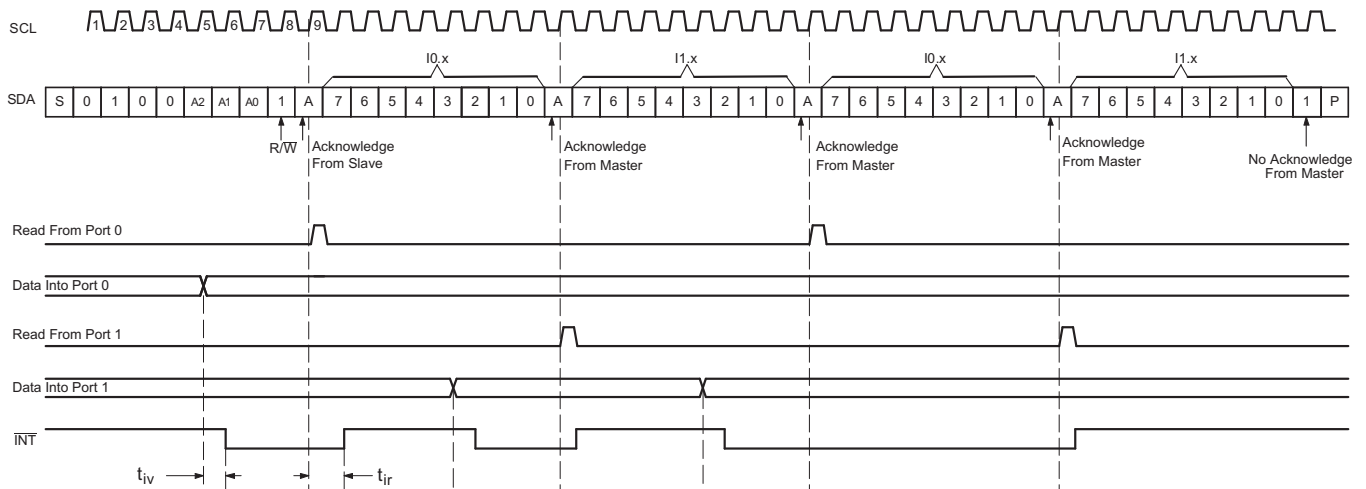


Figure 29. Read from Register

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, the restart occurs when Input Port 0 is being read. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

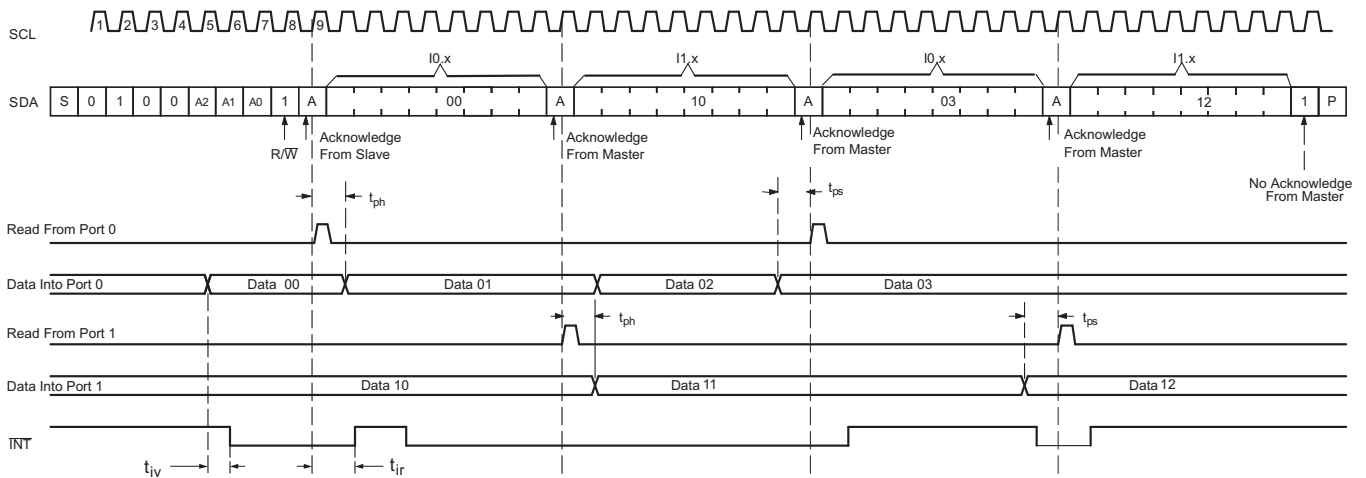
Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

### Programming (continued)



- A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
- B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

**Figure 30. Read Input Port Register, Scenario 1**



- A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).
- B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port.

**Figure 31. Read Input Port Register, Scenario 2**

## Programming (continued)

### 9.5.3 Device Address

Figure 32 shows the address byte of the TCA9555.

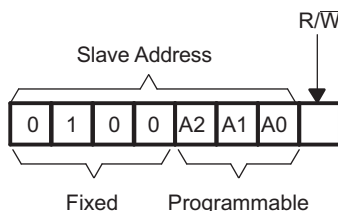


Figure 32. TCA9555 Address

Table 2 shows the TCA9555 address reference.

Table 2. Address Reference

INPUTS			I <sup>2</sup> C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 0x20 (hexadecimal)
L	L	H	33 (decimal), 0x21 (hexadecimal)
L	H	L	34 (decimal), 0x22 (hexadecimal)
L	H	H	35 (decimal), 0x23 (hexadecimal)
H	L	L	36 (decimal), 0x24 (hexadecimal)
H	L	H	37 (decimal), 0x25 (hexadecimal)
H	H	L	38 (decimal), 0x26 (hexadecimal)
H	H	H	39 (decimal), 0x27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

### 9.5.4 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte shown in Table 3, that is stored in the control register in the TCA9555. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that is affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

When a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Figure 33 shows the control register bits.

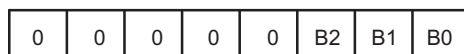


Figure 33. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read-write byte	1111 1111
0	1	1	0x03	Output Port 1	Read-write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read-write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read-write byte	0000 0000

**Table 3. Command Byte (continued)**

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
1	1	0	0x06	Configuration Port 0	Read-write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read-write byte	1111 1111

## 9.6 Register Maps

### 9.6.1 Register Descriptions

The Input Port registers (registers 0 and 1) shown in [Table 4](#) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I<sup>2</sup>C device that the Input Port register is accessed next.

**Table 4. Registers 0 and 1 (Input Port Registers)**

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) shown in [Table 5](#) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

**Table 5. Registers 2 and 3 (Output Port Registers)**

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) shown in [Table 6](#) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

**Table 6. Registers 4 and 5 (Polarity Inversion Registers)**

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) shown in [Table 7](#) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 7. Registers 6 and 7 (Configuration Registers)**

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1





## Typical Application (continued)

### 10.2.1 Design Requirements

The designer must take into consideration the system, to be sure not to violate any of the parameters. [Table 8](#) shows some key parameters which must not be violated.

**Table 8. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
I <sup>2</sup> C and Subsystem Voltage (V <sub>CC</sub> )	5 V
Output current rating, P-port sinking (I <sub>OL</sub> )	25 mA
I <sup>2</sup> C bus clock (SCL) speed	400 kHz

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 Calculating Junction Temperature and Power Dissipation

When designing with this device, it is important that the [Recommended Operating Conditions](#) not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in [Equation 1](#).

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

$\theta_{JA}$  is the standard junction to ambient thermal resistance measurement of the package, as seen in the [Thermal Information](#) table.  $P_d$  is the total power dissipation of the device, and the approximation is shown in [Equation 2](#).

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

[Equation 2](#) is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the INT and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using [Equation 3](#) to calculate the power dissipation in INT or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

[Equation 3](#) shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the  $V_{OL}$  of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

[Equation 4](#) shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between  $V_{CC}$  and the output voltage).

#### 10.2.2.2 Minimizing I<sub>CC</sub> When I/O Is Used to Control LED

When an I/O is used to control an LED, normally it is connected to  $V_{CC}$  through a resistor as shown in [Figure 34](#). Because the LED acts as a diode, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The  $\Delta I_{CC}$  parameter in the [Electrical Characteristics](#) table shows how  $I_{CC}$  increases as  $V_{IN}$  becomes lower than  $V_{CC}$ . For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to  $V_{CC}$  when the LED is off to minimize current consumption.

[Figure 35](#) shows a high-value resistor in parallel with the LED. [Figure 36](#) shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevent additional supply current consumption when the LED is off.

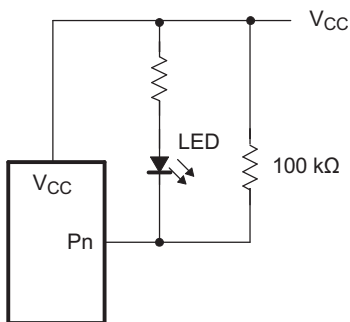


Figure 35. High-Value Resistor in Parallel With LED

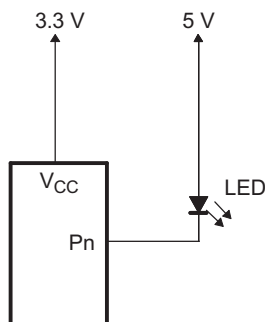


Figure 36. Device Supplied by Lower Voltage

10.2.2.3 Pull-Up Resistor Calculation

The pull-up resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in Equation 5.

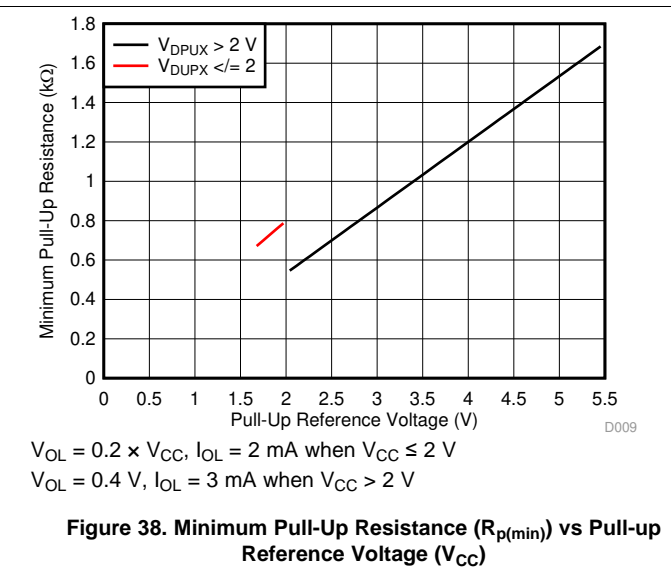
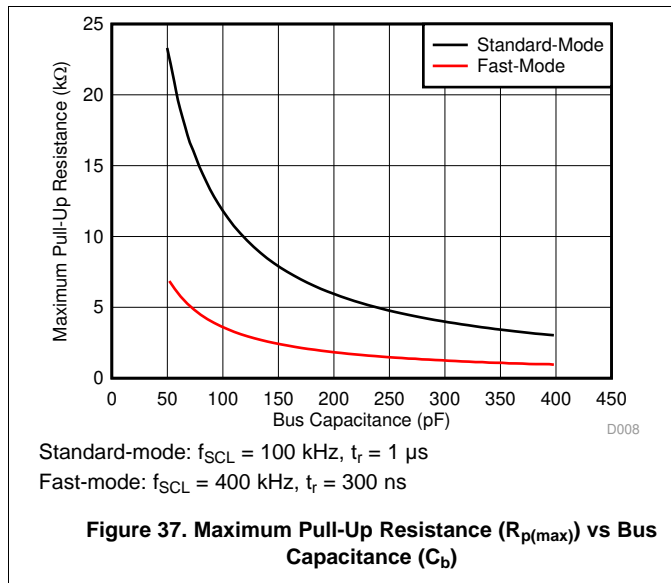
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{5}$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{6}$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9555,  $C_i$  for SCL or  $C_{io}$  for SDA, the capacitance of wires, connections and traces, and the capacitance of additional slaves on the bus. For further details, see the I<sup>2</sup>C Pull-up Resistor Calculation application report, SLVA689.

**10.2.3 Application Curves**



## 11 Power Supply Recommendations

In the event of a glitch (data output or input or even power) or data corruption, the TCA9555 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 39 and Figure 40.

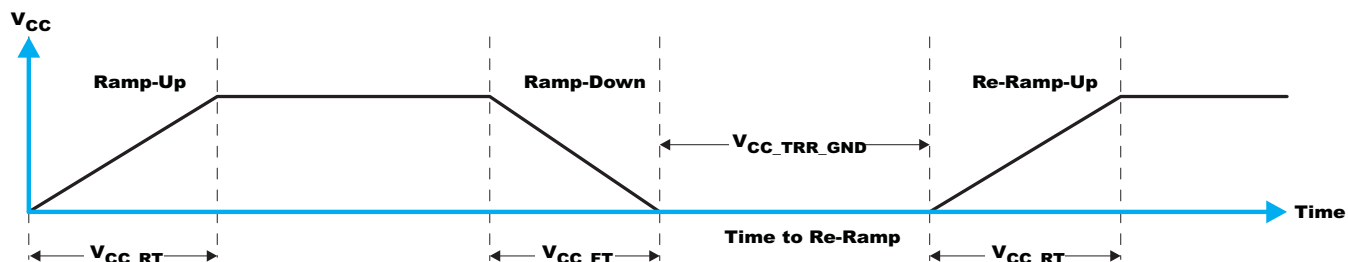


Figure 39.  $V_{CC}$  is Lowered Below 0.2 V or 0 V and Then Ramped Up to  $V_{CC}$

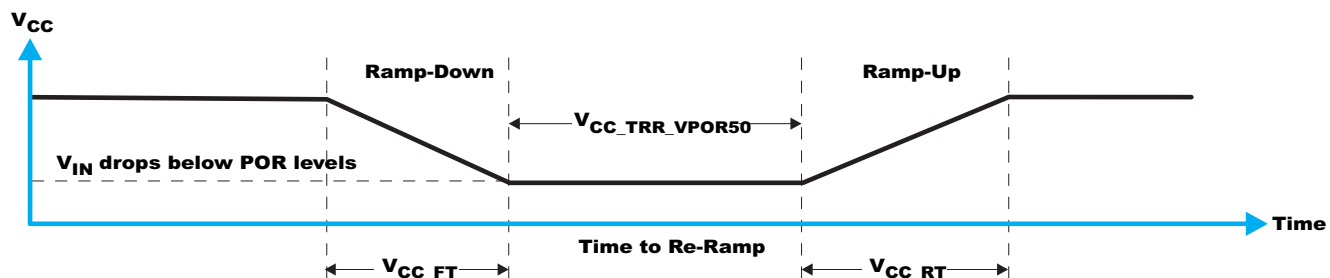


Figure 40.  $V_{CC}$  is Lowered Below the POR Threshold, Then Ramped Back Up to  $V_{CC}$

Table 9 specifies the performance of the power-on reset feature for TCA9555 for both types of power-on reset.

Table 9. RECOMMENDED SUPPLY SEQUENCING AND RAMP RATES<sup>(1)</sup>

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate of $V_{CC}$	See Figure 39	0.1		2000	ms
$V_{CC\_RT}$	Rise rate of $V_{CC}$	See Figure 39	0.1		2000	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See Figure 39	1			$\mu$ s
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)	See Figure 40	1			$\mu$ s
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW}$	See Figure 41			1.2	V
$V_{CC\_MV}$	The minimum voltage that $V_{CC}$ can glitch down to without causing a reset ( $V_{CC\_GH}$ must also not be violated)	See Figure 41	1.5			V
$V_{CC\_GW}$	Glitch width that does not cause a functional disruption	See Figure 41			10	$\mu$ s

(1)  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 41 and Table 9 provide more information on how to measure these specifications.

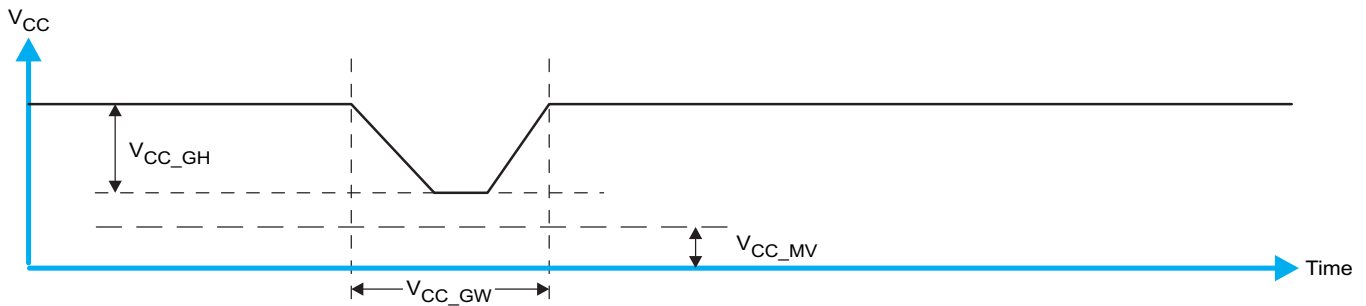


Figure 41. Glitch Width and Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 42 and Table 9 provide more details on this specification.

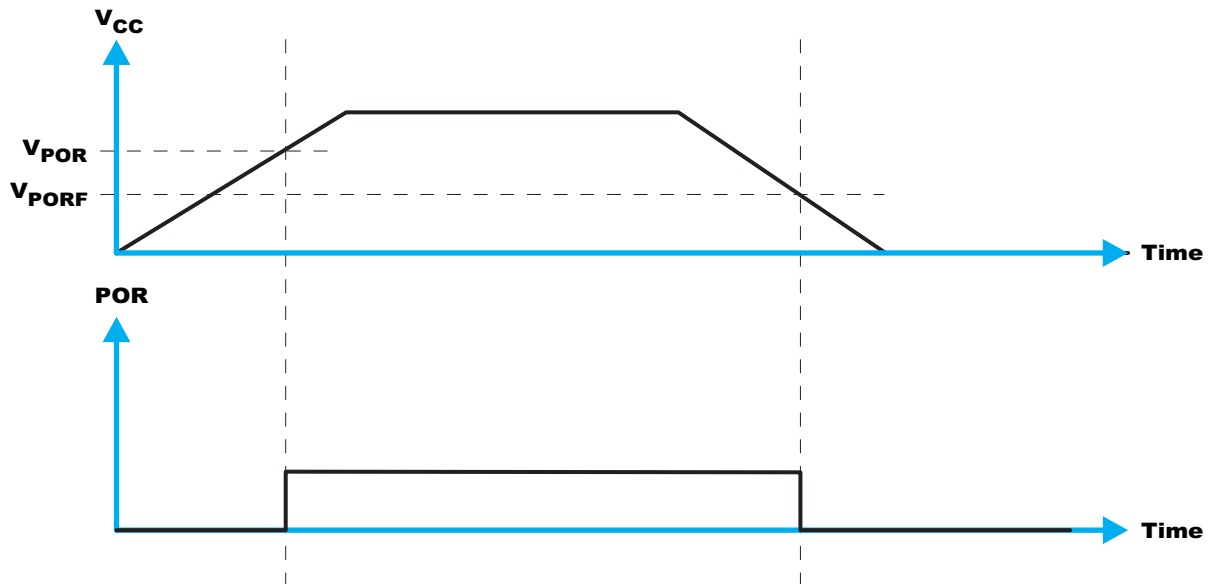


Figure 42.  $V_{POR}$

## 12 Layout

### 12.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9555, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V<sub>CC</sub> pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9555 as possible. These best practices are shown in the *Layout Example*.

For the layout example provided in the *Layout Example*, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub>, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in the *Layout Example*.

### 12.2 Layout Example

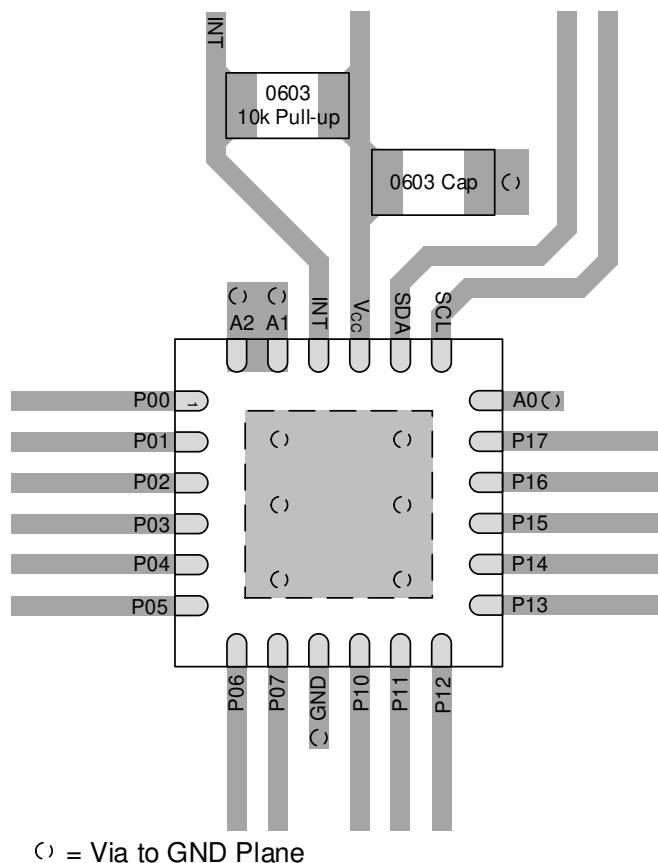


Figure 43. TCA9555 Layout Example

## 13 デバイスおよびドキュメントのサポート

### 13.1 ドキュメントのサポート

#### 13.1.1 関連資料

関連資料については、以下を参照してください。

- 『I2Cのプルアップ抵抗値の計算』、[SLVA689](#)
- 『リピータを使用するI2Cバスの最大クロック周波数』、[SLVA695](#)
- 『ロジックの概要』、[SLVA700](#)
- 『I2Cバスについて理解する』、[SLVA704](#)
- 『IO エクспанダ EVM ユーザー・ガイド』、[SLVUA59A](#)

#### 13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

#### 13.3 コミュニティ・リソース

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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#### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9555DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD9555	<a href="#">Samples</a>
TCA9555DBT	ACTIVE	SSOP	DB	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD9555	<a href="#">Samples</a>
TCA9555PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW555	<a href="#">Samples</a>
TCA9555RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TD9555	<a href="#">Samples</a>
TCA9555RTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW555	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9555DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TCA9555DBT	SSOP	DB	24	250	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TCA9555PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9555RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCA9555RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCA9555RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9555DBR	SSOP	DB	24	2000	356.0	356.0	35.0
TCA9555DBT	SSOP	DB	24	250	356.0	356.0	35.0
TCA9555PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
TCA9555RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TCA9555RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
TCA9555RTWR	WQFN	RTW	24	3000	356.0	356.0	35.0

## GENERIC PACKAGE VIEW

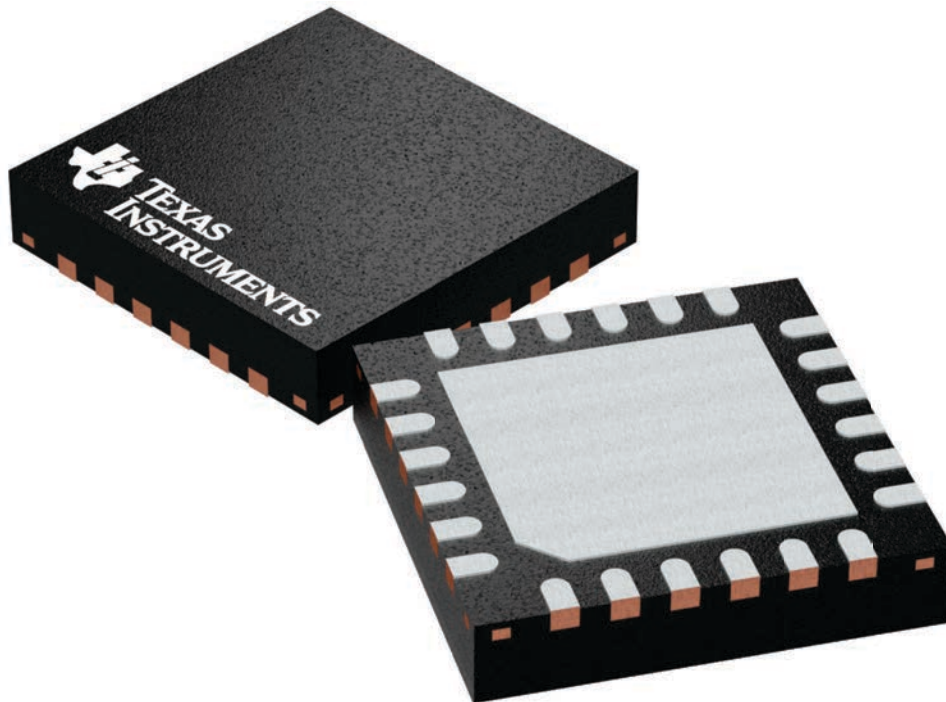
**RTW 24**

**WQFN - 0.8 mm max height**

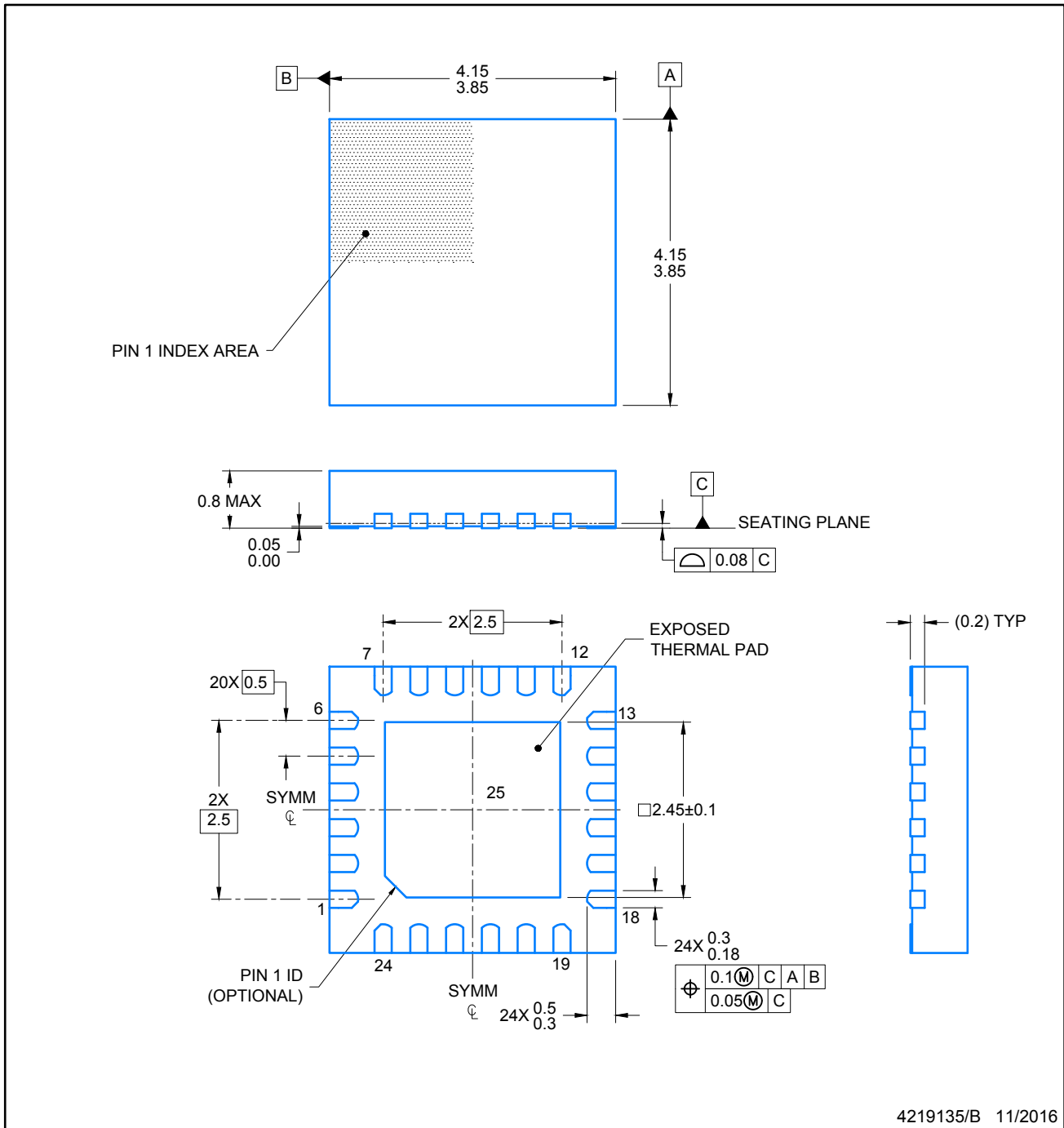
4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



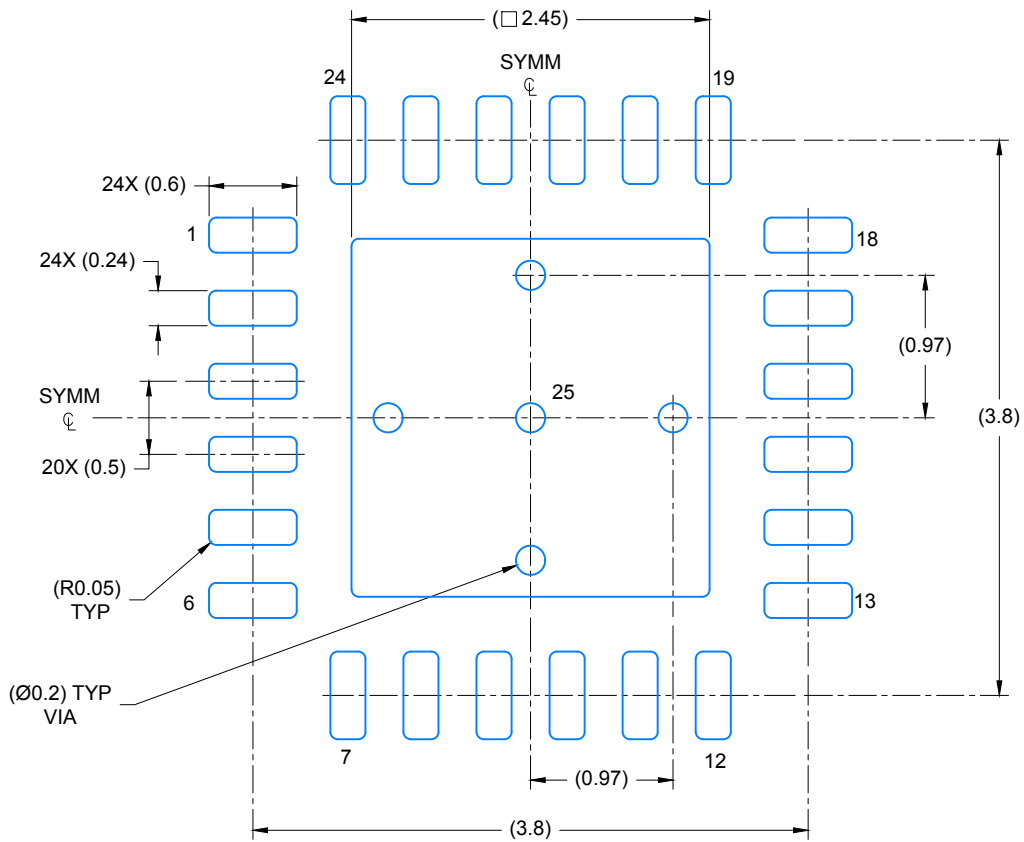
4224801/A



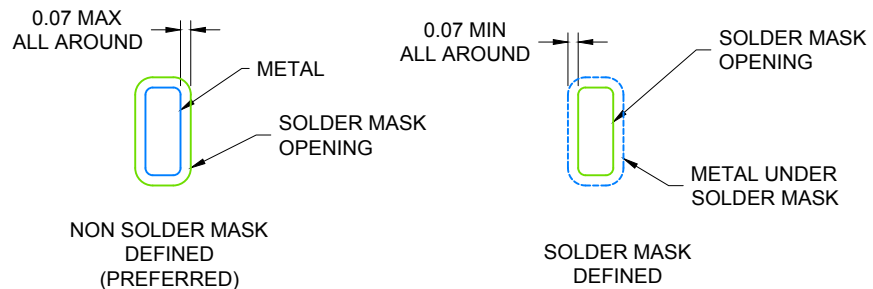
4219135/B 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
SCALE: 20X

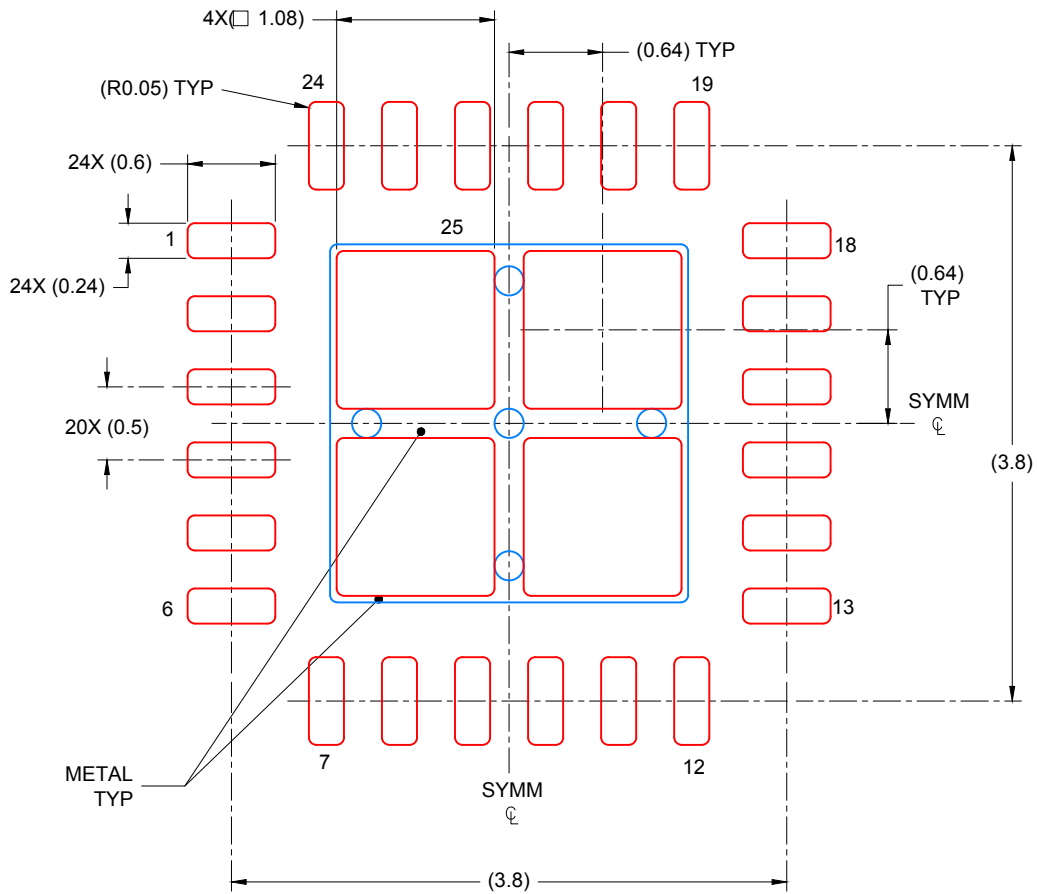


SOLDER MASK DETAILS

4219135/B 11/2016

NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:  
 78% PRINTED COVERAGE BY AREA UNDER PACKAGE  
 SCALE: 20X

4219135/B 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

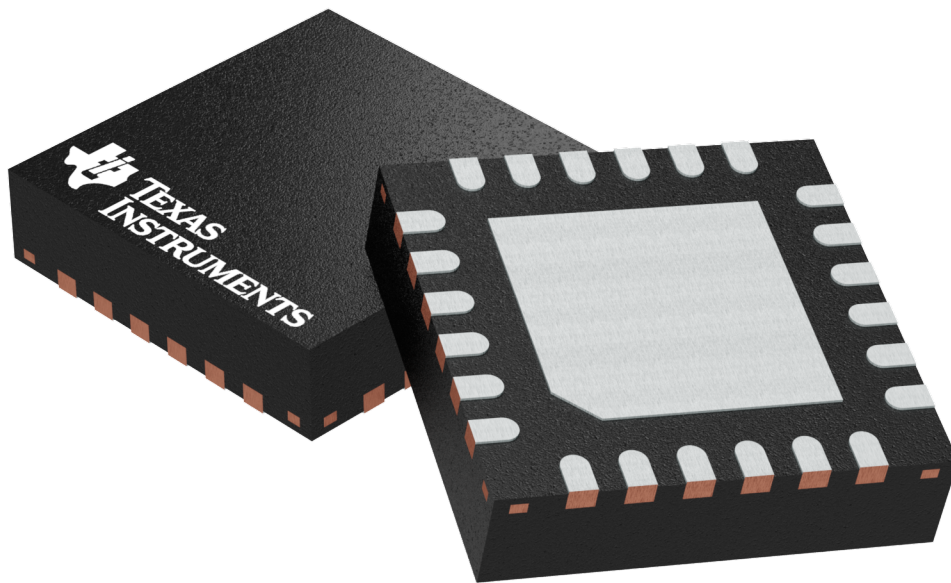
4040065 /E 12/01

**RGE 24**

**GENERIC PACKAGE VIEW**

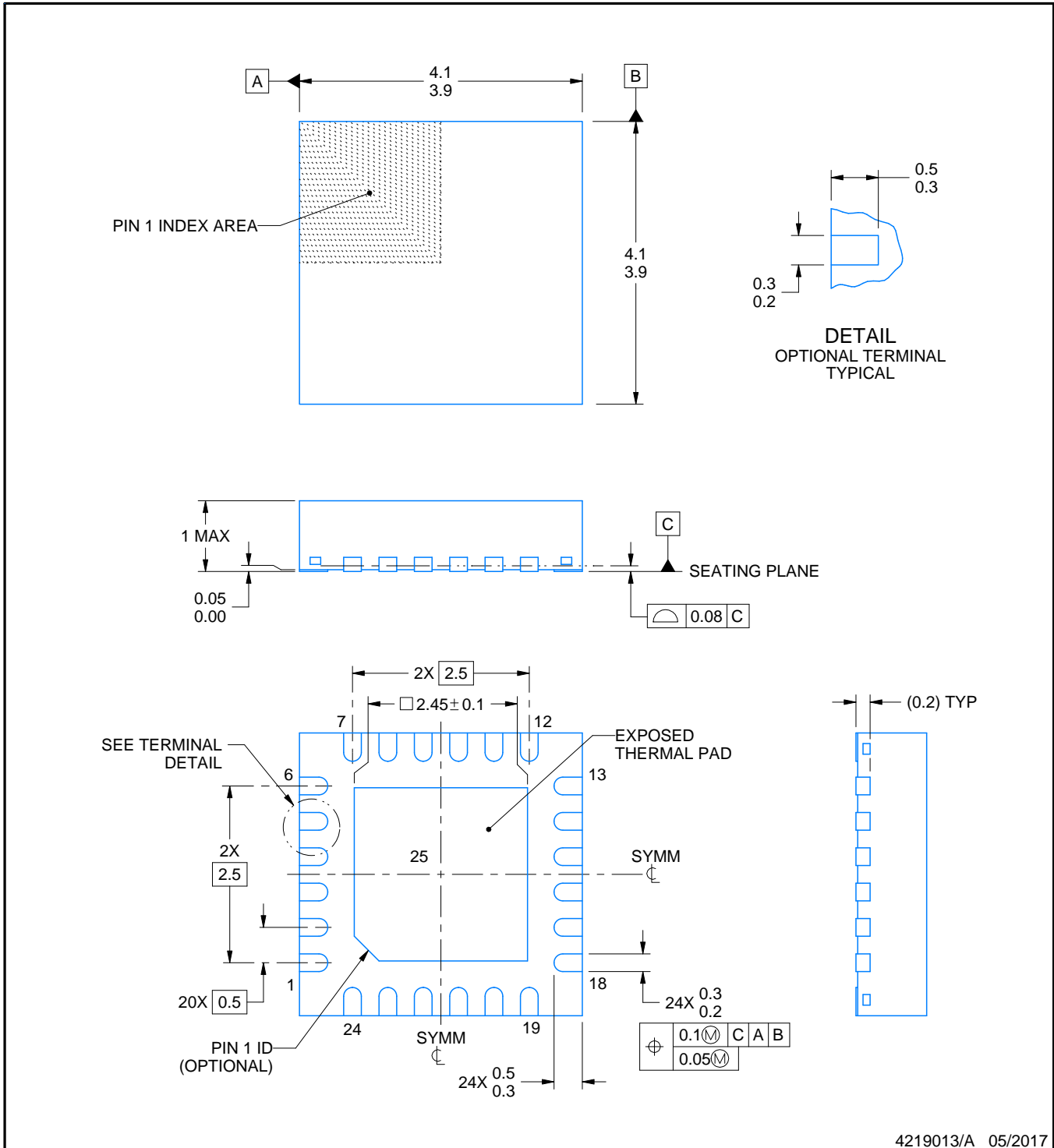
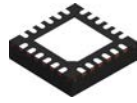
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



4219013/A 05/2017

NOTES:

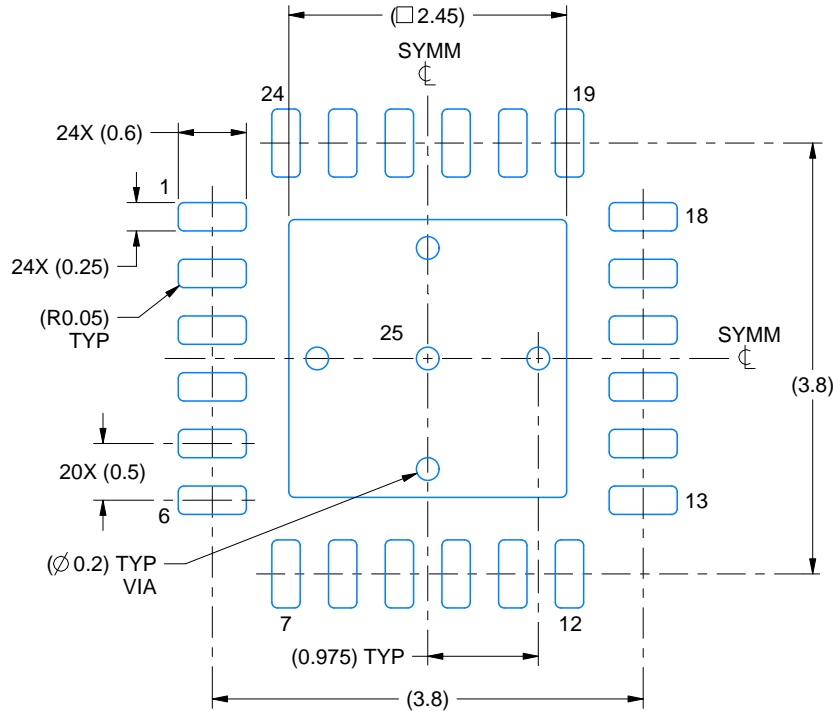
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

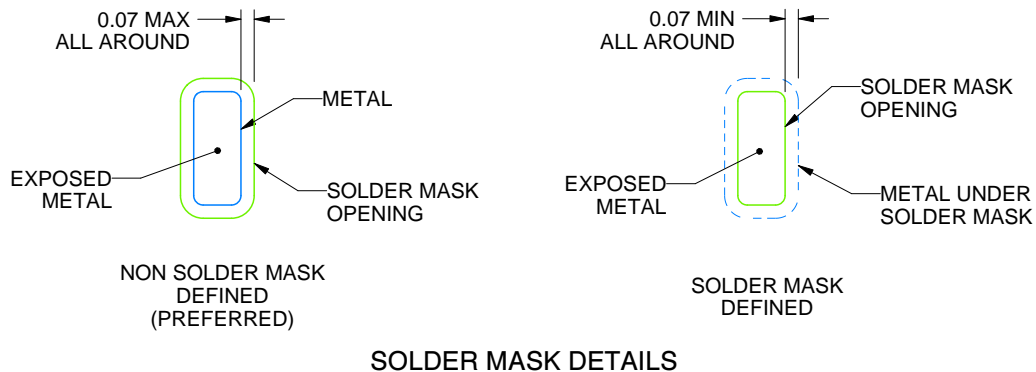
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

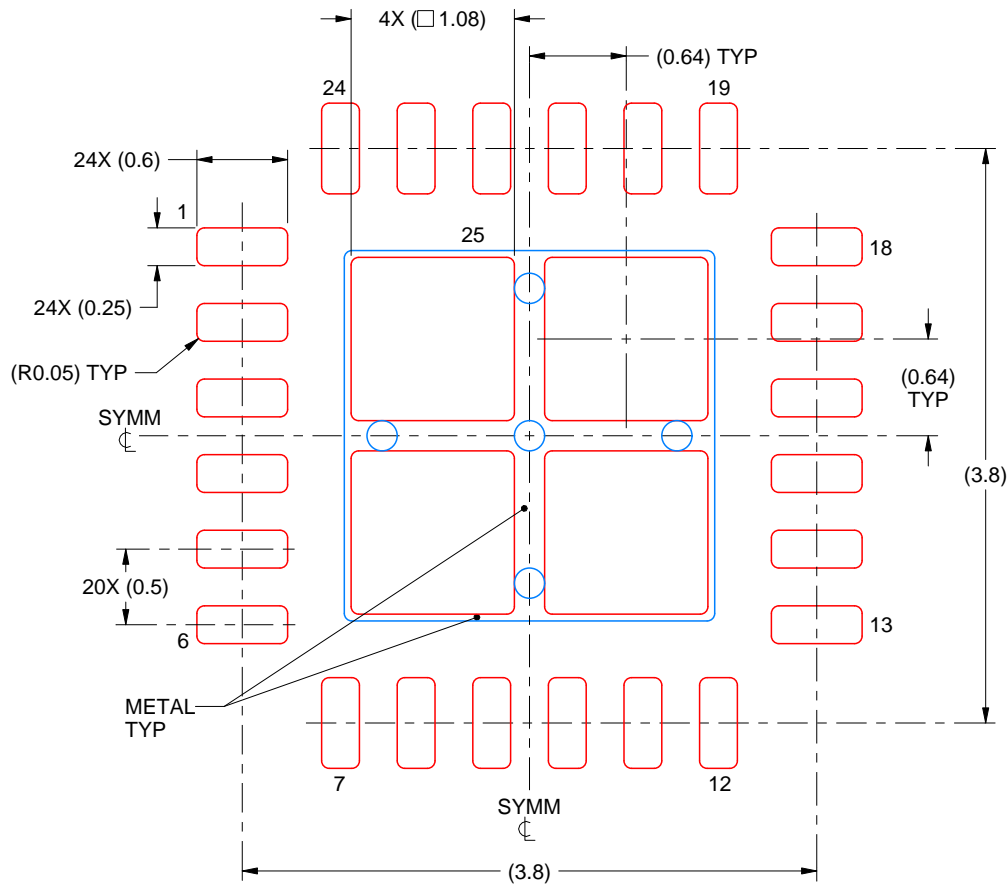
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

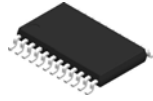
EXPOSED PAD 25  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

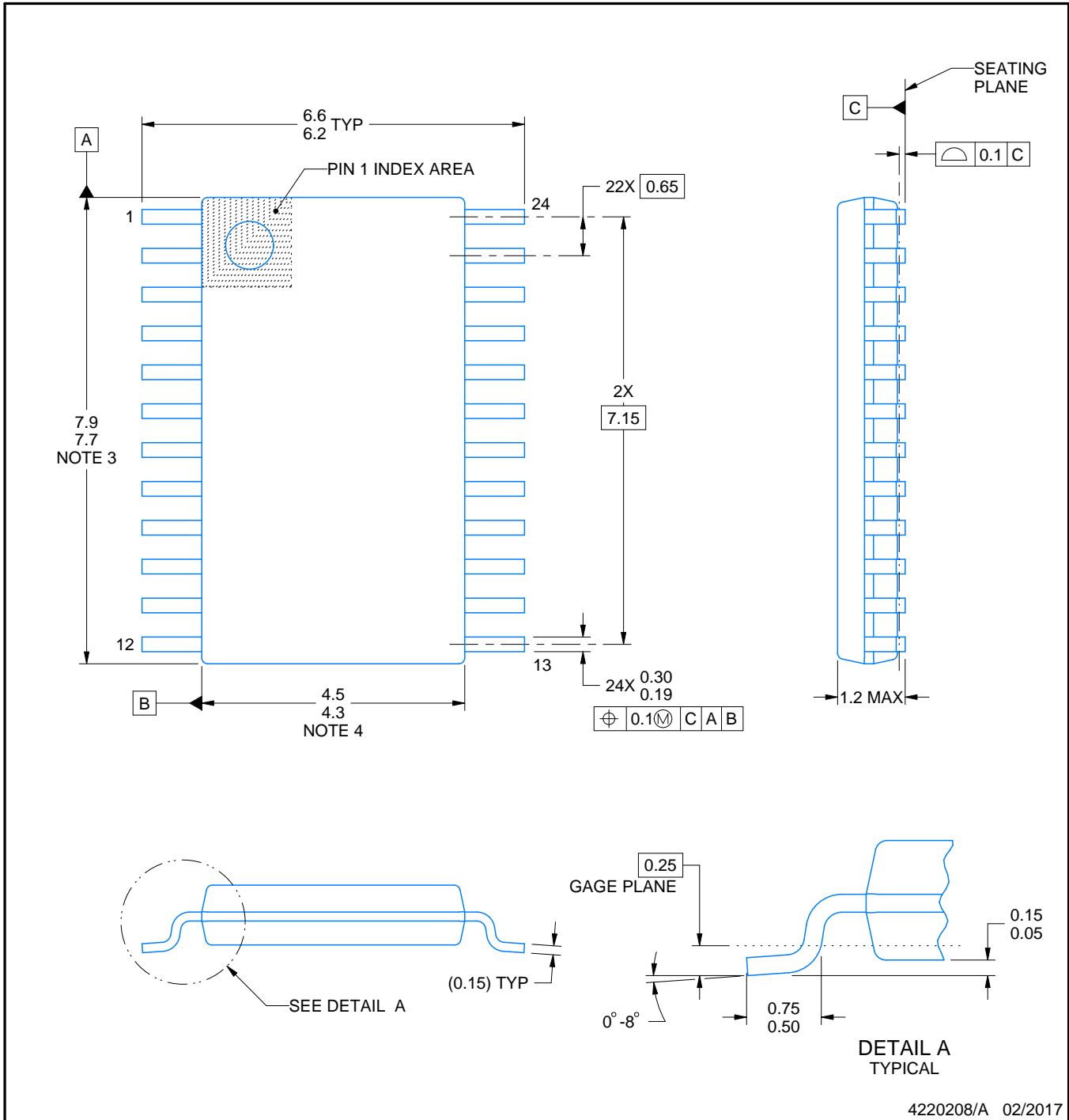
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

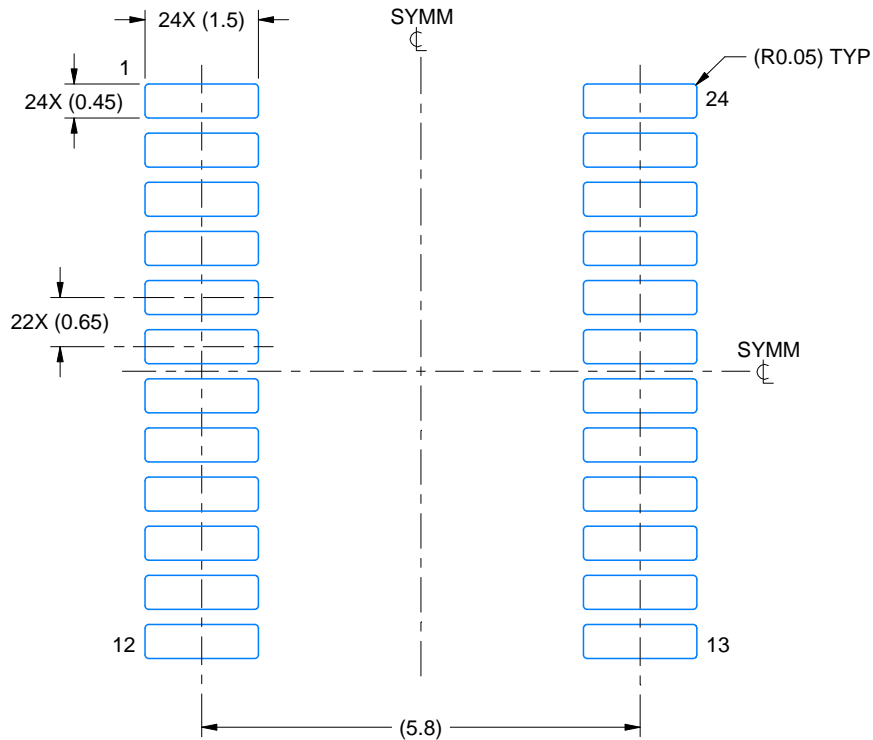
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

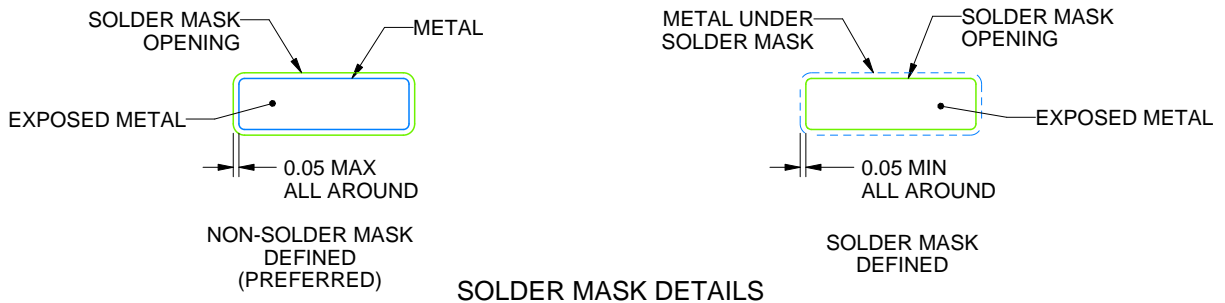
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

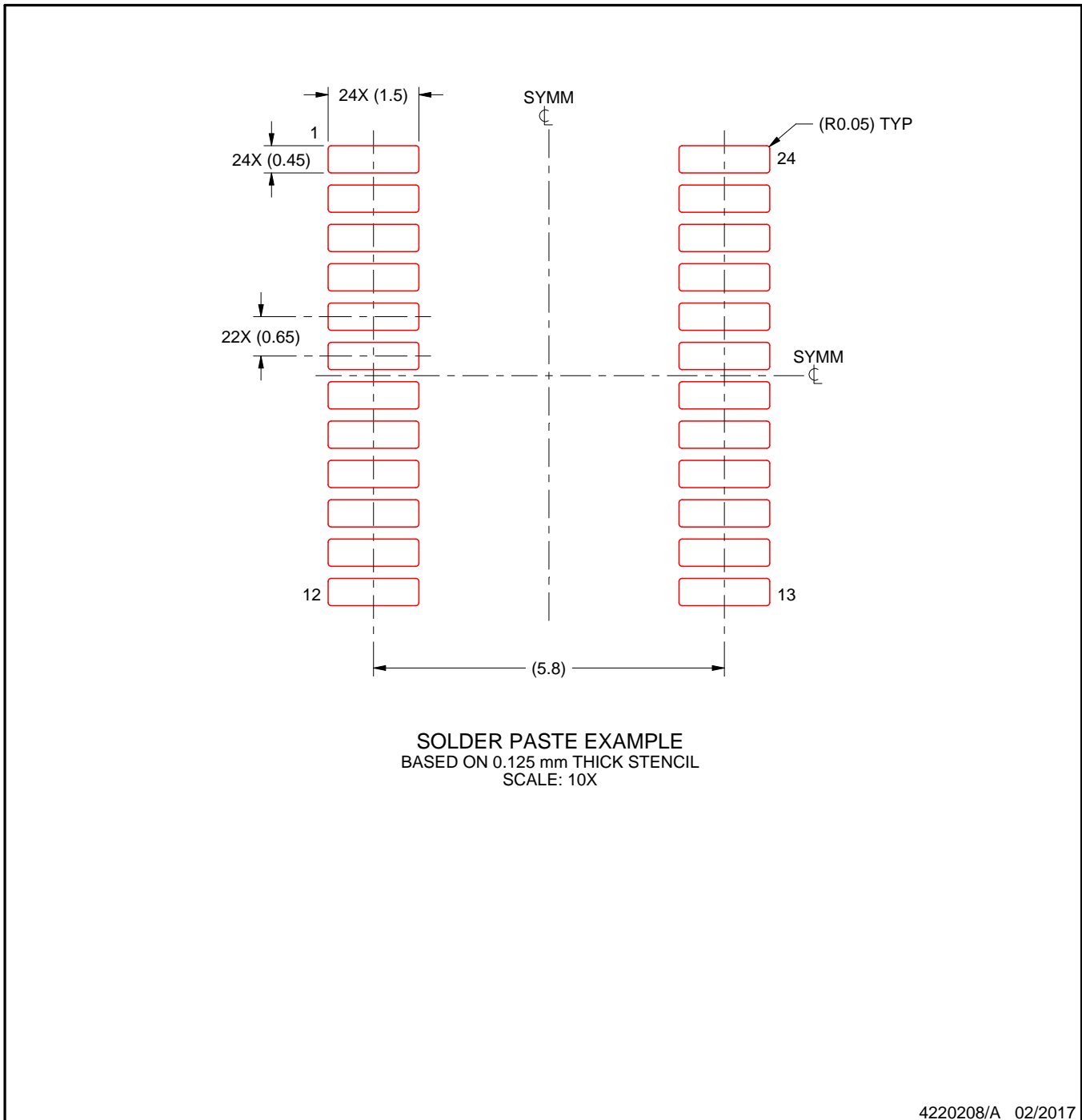
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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