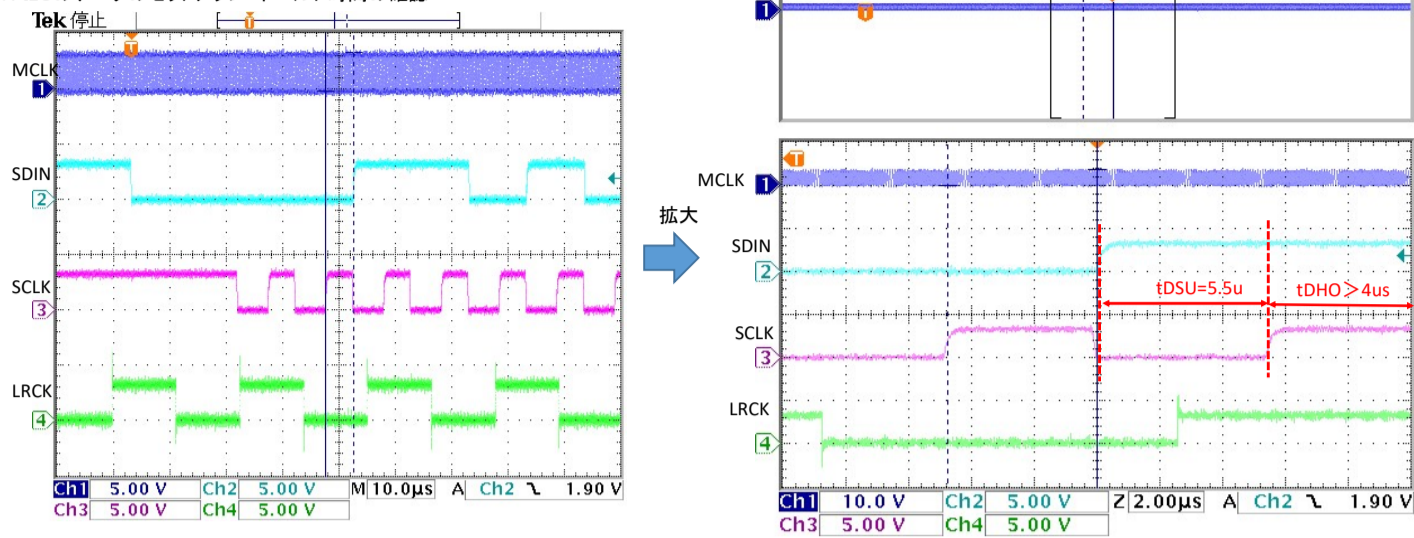


1. I2Cのデータのセットアップ・ホールド時間の確認



CONTROL INTERFACE TIMING – 3-WIRE MODE

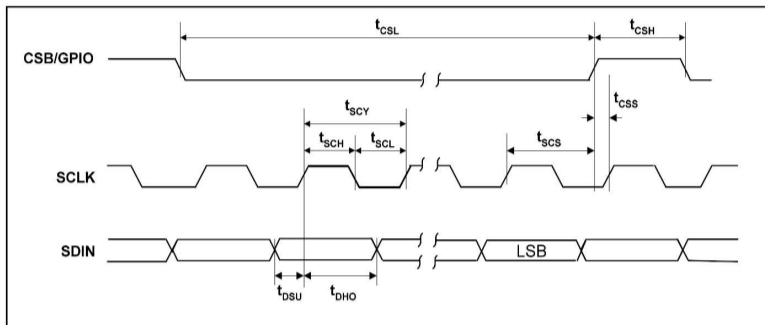


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

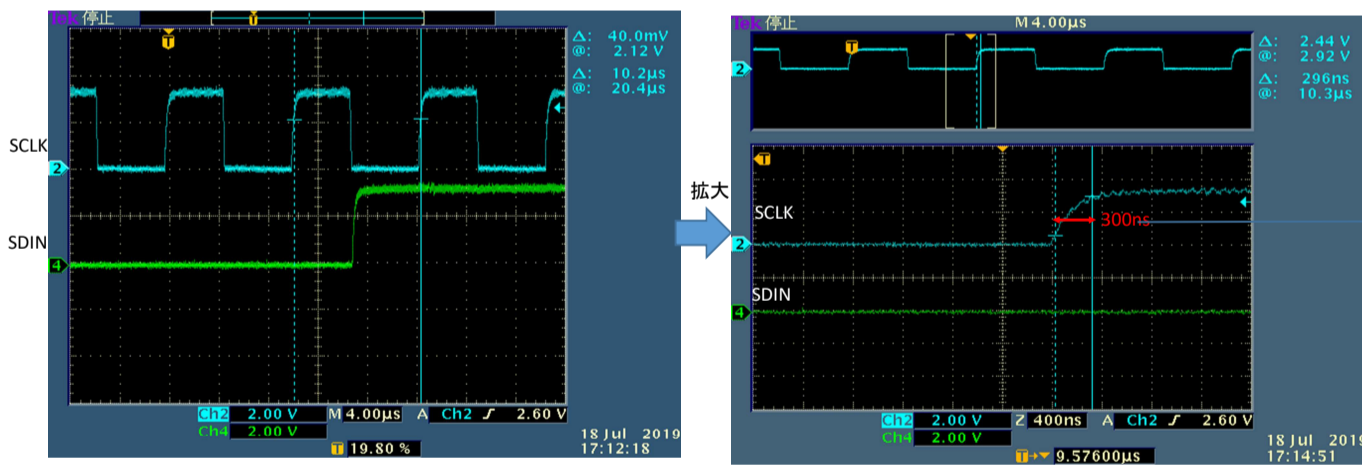
Test Conditions

DCVDD = 1.8V, DBVDD = AVDD = SPKVDD = 3.3V, DGND = AGND = SPKGND = 0V, TA = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Program Register Input Information</b>					
SCLK rising edge to CSB rising edge	$t_{SCS}$	80			ns
SCLK pulse cycle time	$t_{SCY}$	200			ns
SCLK pulse width low	$t_{SCL}$	80			ns
SCLK pulse width high	$t_{SCH}$	80			ns
SDIN to SCLK set-up time	$t_{DSU}$	40			ns
SCLK to SDIN hold time	$t_{DHO}$	40			ns
CSB pulse width low	$t_{CSL}$	40			ns
CSB pulse width high	$t_{CSH}$	40			ns
CSB rising to SCLK rising	$t_{CSS}$	40			ns
Pulse width of spikes that will be suppressed	$t_{ps}$	0		5	ns

⇒5.5us OK  
⇒4us以上 OK

2. I2Cのクロックの立ち上がり確認



下図のWM8971のタイミングチャートによると、SCLKの立ち上がりはmax300nsとあります。実測波形ではほぼ300nsです。

WM8971のI2Cのタイミング

CONTROL INTERFACE TIMING – 2-WIRE MODE

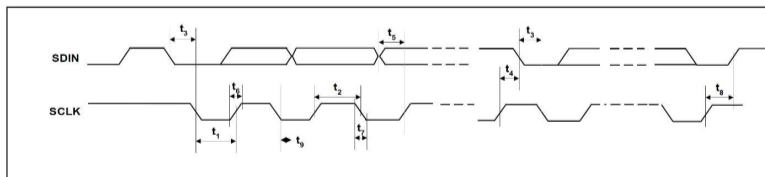


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, TA=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
<b>Program Register Input Information</b>					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	$t_1$	1.3			us
SCLK High Pulse-Width	$t_2$	600			ns
Hold Time (Start Condition)	$t_3$	600			ns
Setup Time (Start Condition)	$t_4$	600			ns
Data Setup Time	$t_5$	100			ns
SDIN, SCLK Rise Time	$t_6$			300	ns
SDIN, SCLK Fall Time	$t_7$			300	ns
Setup Time (Stop Condition)	$t_8$	600			ns
Data Hold Time	$t_9$			900	ns
Pulse width of spikes that will be suppressed	$t_{ps}$	0		5	ns

⇒約300ns